

PCH_IBEX GPIO	PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
	GPIO 00	Native	NA	-	+3VS
	GPIO 01	GPO	NA	INT TBD	+3VS
	GPIO [2:5]	Native	PCI_INTE#~H#	8.2K EXT PU	+3VS
	GPIO 06	GPO	NA	10K @	+3VS
	GPIO 07	GPO	NA	INT TBD	+3VS
	GPIO 08	GPI	EXT_SMI#	10K EXT PU & INT PU	+3VSUS
	GPIO 09	Native	USB_OC5#	10K EXT PU(not used)	+3VSUS
	GPIO 10	Native	USB_OC6#	10K EXT PU(not used)	+3VSUS
	GPIO 11	GPI	EXT_SCI#	10K EXT PU	+3VSUS
	GPIO 12	GPO	TP /PM_LANPHY_EN	-	+3VSUS
	GPIO 13	GPO	NA	-	+3VSUS
	GPIO 14	Native	USB_OC7#	10K EXT PU(not used)	+3VSUS
	GPIO 15	GPO	NA	INT PD	+3VSUS
	GPIO 16	GPO	NA	10K @ EXT PU	+3VS
	GPIO 17	GPI	NA	10K @ EXT PD & INT PD	+3VS
	GPIO 18	GPO	CLKREQ1_TV#	10K EXT PU(no device)	+3VS
	GPIO 19	Native	SATA1GP	10K @ EXT PU	+3VS
	GPIO 20	Native	CLK_WLAN_REQ#_R	10K EXT PD	+3VS
	GPIO 21	Native	SATA0GP	10K @ EXT PU	+3VS
	GPIO 22	GPO	NA	-	+3VS
	GPIO 23	GPO	NA	INT PU	+3VS
	GPIO 24	GPO	NA	-	+3VSUS
	GPIO 25	GPO	TP /CLKREQ3_NEWCARD#	10K EXT PU(no device)	+3VSUS
	GPIO 26	GPO	CLK_REQ4#	10K EXT PU(no device)	+3VSUS
	GPIO 27	GPO	NA	INT WEAK PU	+3VSUS
	GPIO 28	GPO	WLAN_ON	-	+3VSUS
	GPIO 29	GPO	NA	-	+3VSUS
	GPIO 30	GPO	ME_SUSPWRDNACK	10K EXT PU	+3VSUS
	GPIO 31	Native	NA	-	+3VSUS
	GPIO 32	Native	PM_CLKRUN#	8.2K EXT PU	+3VS
	GPIO 33	GPO	HDA_DOCK_EN#	1K @ EXT PD	+3VS
	GPIO 34	GPO	NA	-	+3VS
	GPIO 35	Native	SATA_CLK_REQ#	10K EXT PD	+3VS
	GPIO 36	GPO	DGPU_PWR_EN#	10K @ EXT PD	+3VS
	GPIO 37	GPI	DGPU_PRSENT#	10K EXT PU	+3VS
	GPIO 38	GPO	NA	-	+3VS
	GPIO 39	GPO	NA	-	+3VS
	GPIO 40	Native	USB_OC1#	10K EXT PU(Not used)	+3VSUS
	GPIO 41	Native	USB_OC2#	10K EXT PU(Not used)	+3VSUS
	GPIO 42	Native	USB_OC3#	10K EXT PU(Not used)	+3VSUS
	GPIO 43	Native	USB_OC4#	10K EXT PU(Not used)	+3VSUS
	GPIO 44	GPO	CLKREQ5_CR#	10K EXT PU(no device)	+3VSUS
	GPIO 45	GPO	CLK_REQ6#	-	+3VSUS
	GPIO 46	GPO	RST_GATE	10K EXT PU	+3VSUS
	GPIO 47	Native	CLKREQ_PEG#	10K EXT PU	+3VSUS
	GPIO 48	GPO	NA	10K @ EXT PU	+3VS
	GPIO 49	Native	PCH_ALERT#	-	+3VS
	GPIO 50	GPO	PCI_REQ1#	8.2K EXT PU	+3VS
	GPIO 51	GPO	PCI_GNT1#	1K @ EXT PD	+3VS
	GPIO 52	GPO	PCI_REQ2#	8.2K EXT PU	+5VS
	GPIO 53	GPO	PCI_GNT2#	-	+3VS
	GPIO 54	Native	PCI_REQ3#	8.2K EXT PU	+3VS
	GPIO 55	GPO	PCI_GNT3#	1K @ PD /INT PU	+3VS
	GPIO 56	Native	CLKREQ_LAN#	10K EXT PD	+3VSUS
	GPIO 57	GPO	BT_ON	-	+3VSUS
	GPIO 58	Native	SML1_CLK	4.7K EXT PU	+3VSUS
	GPIO 59	Native	USB_OC0#	10K EXT PU(Not used)	+3VSUS
	GPIO 60	GPO	NA	-	+3VSUS
	GPIO 61	GPO	NA	-	+3VSUS
	GPIO 62	GPO	NA	-	+3VSUS
	GPIO 63	GPO	NA	-	+3VSUS
	GPIO 64	GPO	TP /CLK_OUT0	INT TBD	+3VS
	GPIO 65	GPO	TP /CLK_OUT1	INT TBD	+3VS
	GPIO 66	GPO	TP /CLK_OUT2	INT TBD	+3VS
	GPIO 67	Native	CLK_USB48_CR	INT TBD	+3VS
	GPIO 72	GPO	PM_BATLOW#	8.2K EXT PU	+3VSUS
	GPIO 73	Native	CLK_REQ0#	10K EXT PU (no device)	+3VSUS
	GPIO 74	Native	SML1ALERT#	10K EXT PU	+3VSUS
	GPIO 75	Native	SML1_DAT	4.7K EXT PU	+3VSUS

EC IT8502

EC GPIO

Use As

Signal Name

GPA0	PWR_LED#	
GPA1	NA	
GPA2	PWRSERVE#	
GPA3	BAT_LED_G#	
GPA4	LCD_BL_PWM	
GPA5	FAN0_PWM	
GPA6	NA	
GPA7	NA	
GPB0	NA	
GPB1	NA	
GPB2	KSO16	
GPB3	SMB0_CLK	4.7K EXT PU
GPB4	SMB0_DAT	4.7K EXT PU
GPB5	A20GATE	10K EXT PU
GPB6	RC_IN#	10K EXT PU
GPB7	PM_RSMRST#	10K EXT PD
GPC0	NA	
GPC1	SMB1_CLK	4.7K EXT PU
GPC2	SMB1_DAT	4.7K EXT PU
GPC3	PM_PWRBTN#	
GPC4	AC_IN_OC#	10K EXT PU
GPC5	OP_SD#	
GPC6	BAT1_IN_OC#	47K EXT PU
GPC7	NA	
GPD0	PWRLIMIT#	10K EXT PU
GPD1	PM_SUSC#	100K EXT PD
GPD2	BUF_PLT_RST#	
GPD3	EXT_SCI#	
GPD4	EXT_SMI#	
GPD5	LCD_BACKOFF#	
GPD6	FAN0_TACH	
GPD7	SD_CD#_EC	10K EXT PU
GPE0	VSUS_ON	
GPE1	SUSC_EC#	4.7K EXT PD
GPE2	SUSB_EC#	4.7K EXT PD
GPE3	CPU_VRON	
GPE4	PWR_SW#	
GPE5	NA	
GPE6	LID_SW#	
GPE7	NA	
GPFO	NA	
GPF1	NA	
GPF2	NA	
GPF3	NA	
GPF4	TP_CLK	4.7K EXT PU
GPF5	TP_DAT	4.7K EXT PU
GPF6	THRO_CPU	
GPF7	H_PECI	
GPG0	NA	
GPG1	PM_SUSB#	100K EXT PD
GPG2	NA	
GPG6	NA	
GPH0	PM_CLKRUN#	
GPH1	3G_ON#	
GPH2	GFX_VR_ON	
GPH3	NA	
GPH4	NA	
GPH5	NA	
GPH6	NA	
GPI0	PCH_ALERT#	
GPI1	SUS_PWRGD	
GPI2	ALL_SYSTEM_PWRGD	
GPI3	VRM_PWRGD	
GPI4	GFX_VR	
GPI5	NA	
GPI6	NA	
GPI7	NA	
GPJ0	NA	
GPJ1	PM_PWROK	
GPJ2	NA	
GPJ3	NA	
GPJ4	NA	
GPJ5	HDA_DOCK_EN_C	

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2h)
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010010x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	N/A
PCIE 5	N/A
PCIE 6	LAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	N/A
SATA5	N/A

USB 0	USB Port
USB 1	USB Port
USB 2	NA
USB 3	USB Port
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	Card Reader
USB 9	Multimedia SIM
USB 10	WWAN
USB 11	N/A
USB 12	Bluetooth
USB 13	CMOS Camera

PEGATRON

Title : System Setting

Engineer: Marvin Chen

Size Custom

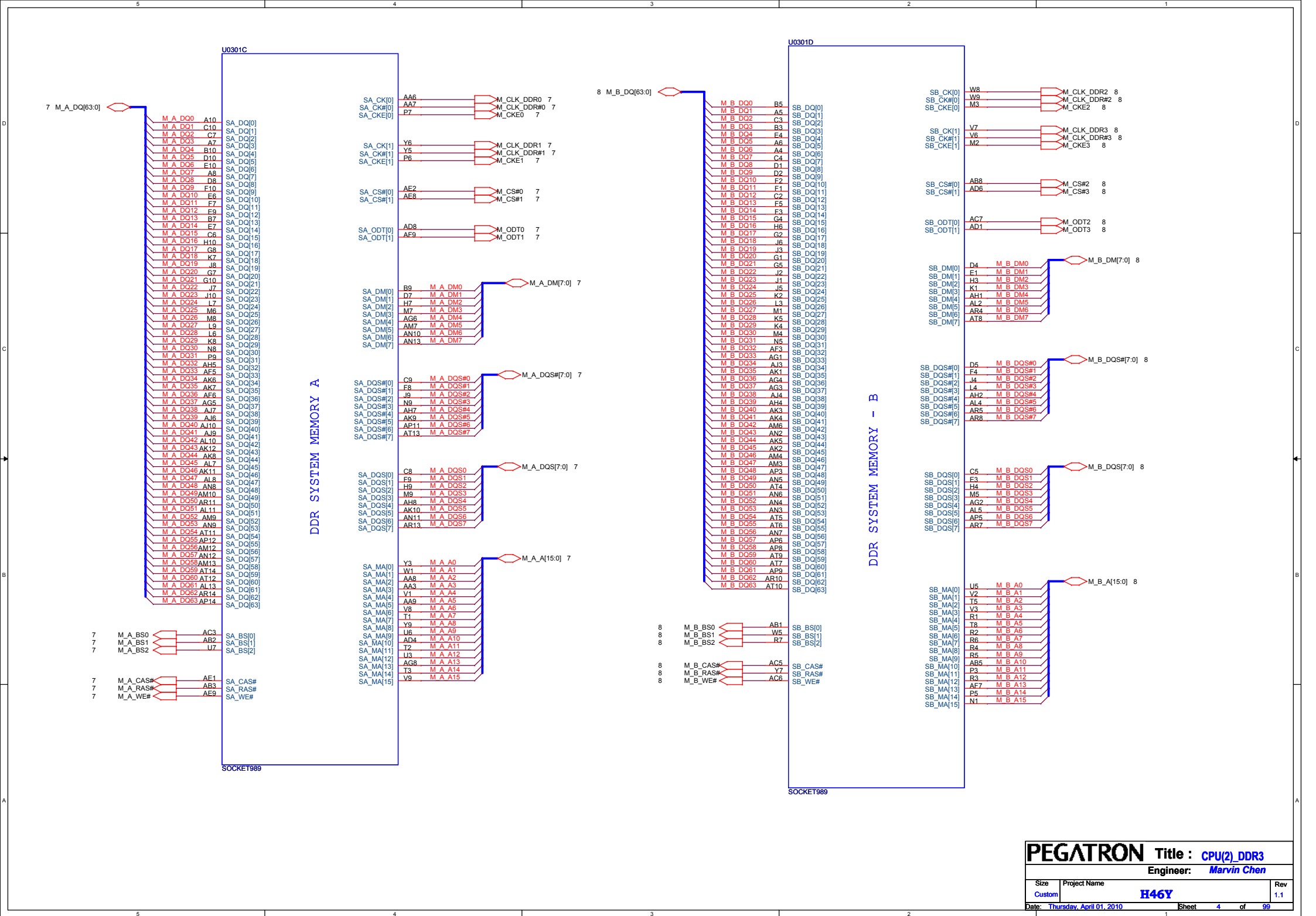
Project Name

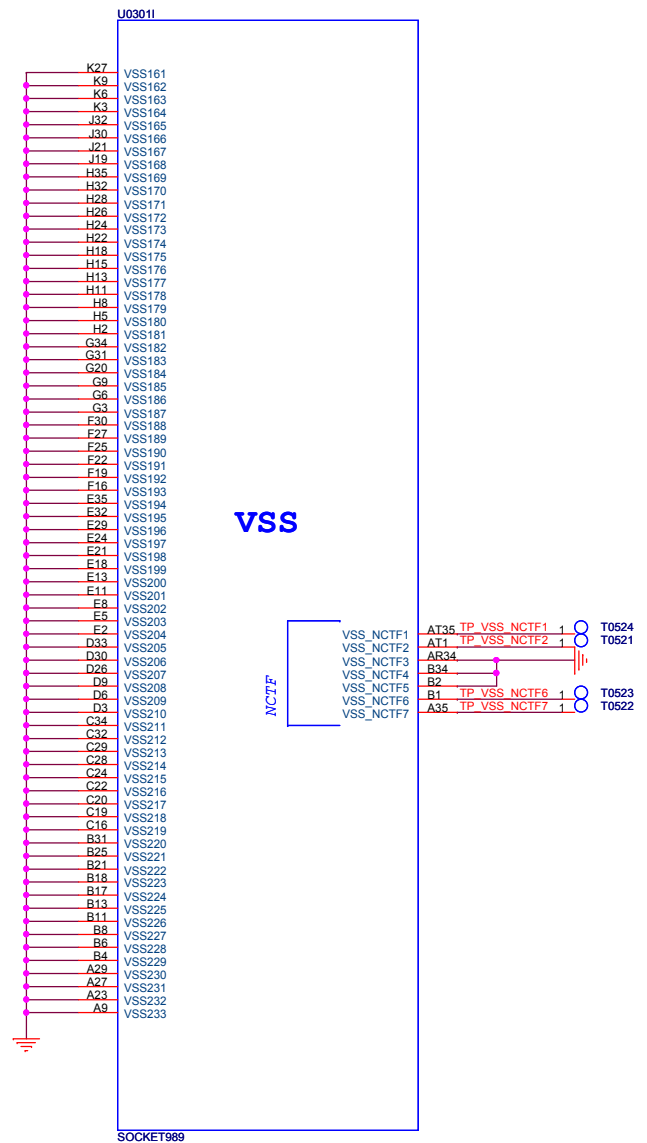
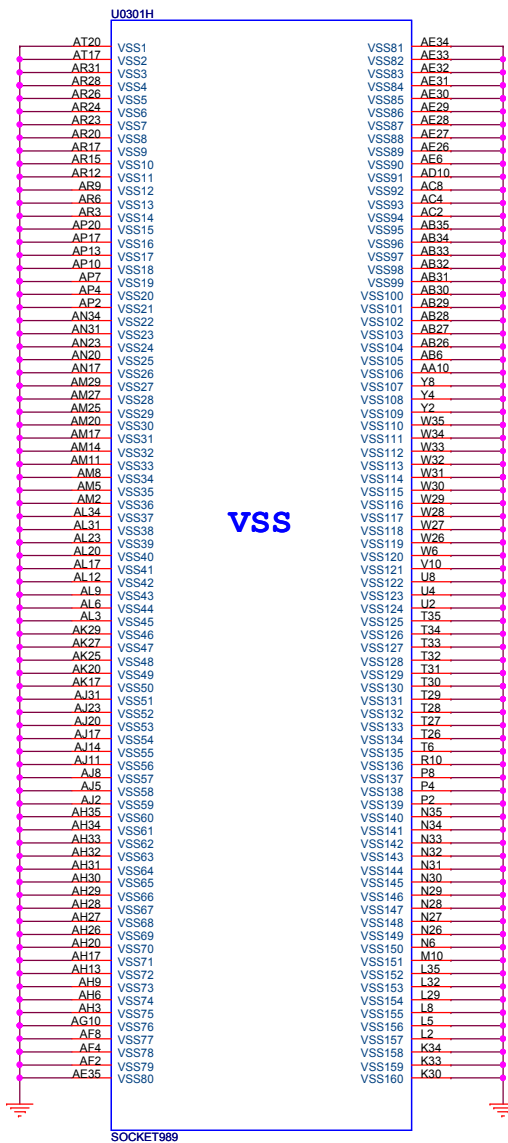
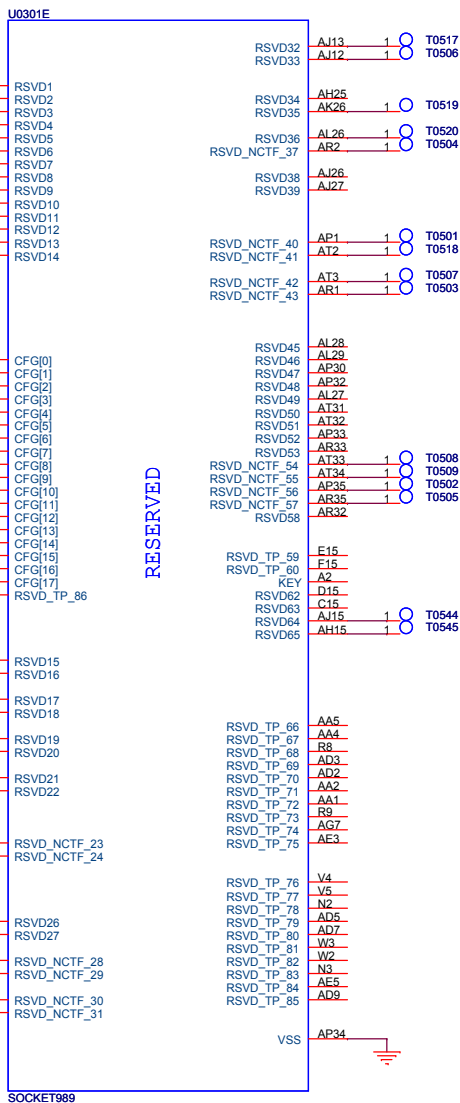
H46Y

Rev 1.1

Date: Thursday, April 01, 2010

Sheet 2 of 99





CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)

- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIe Static Numbering Lane Reversal.(Auburndale Only)

- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)

- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

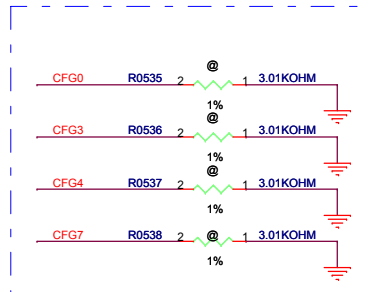
CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)

Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. For a common motherboard design (for AUB and CFD),the pull-down resistor should be used. Does not impact AUB functionality.

Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



PEGATRON Title : CPU(3)_CFG.GND

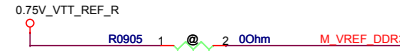
Engineer: Marvin Chen

Size Project Name H46Y Rev 1.1

Date: Thursday, April 01, 2010 Sheet 5 of 99

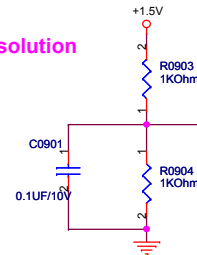
DDR3 Vref

M1: Fixed SO-DIMM VREF_DQ (Default Stuffing)



M2: Programmable SO-DIMM VREF_DQ on motherboard - New Requirement

Note: Use voltage divider instead of I2C solution



M3: Processor Generated SO-DIMM VREFDQ - New Requirement Clarksfield, M3 should be used.

For Arrandale only designs ' Only method M1 should be enabled.

For Clarksfield only designs ' Both M1 AND M3 methods should be enabled simultaneously

For Common Motherboard designs ' Both M1 AND M3 methods should be enabled simultaneously.

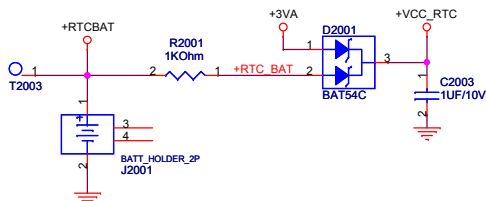
Note:

Please refer to Calpella Mainstream PDG (Doc# 398905) Section 2.5.4 for more details.

M1 - Voltage divider Option

M3 - VREF driven by processor

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



1220-0010000

Strap information:

```
HDA_SPKR: No reboot strap
Low: Disable.
High: Enable
```

HDA DOCK EN#:

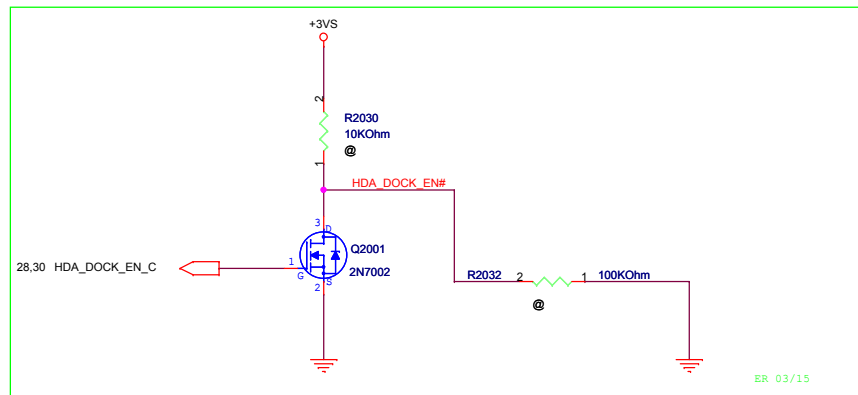
- ```

1.Flash descriptor security:
 Sampled low: override
 Sampled high: in effect.
2.GPIO33 low on the rising edge of PWROK,
 Will also disable Intel ME.

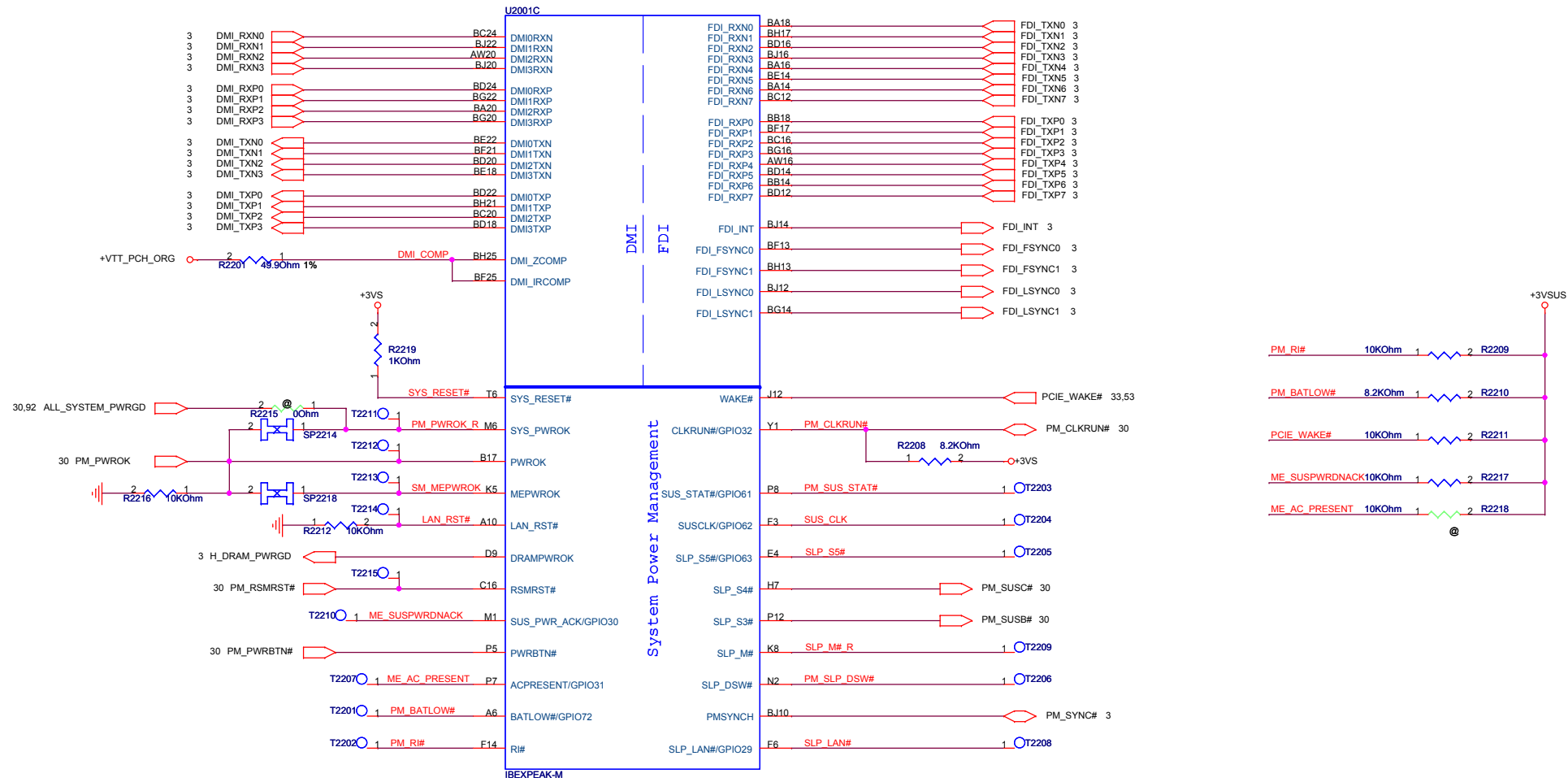
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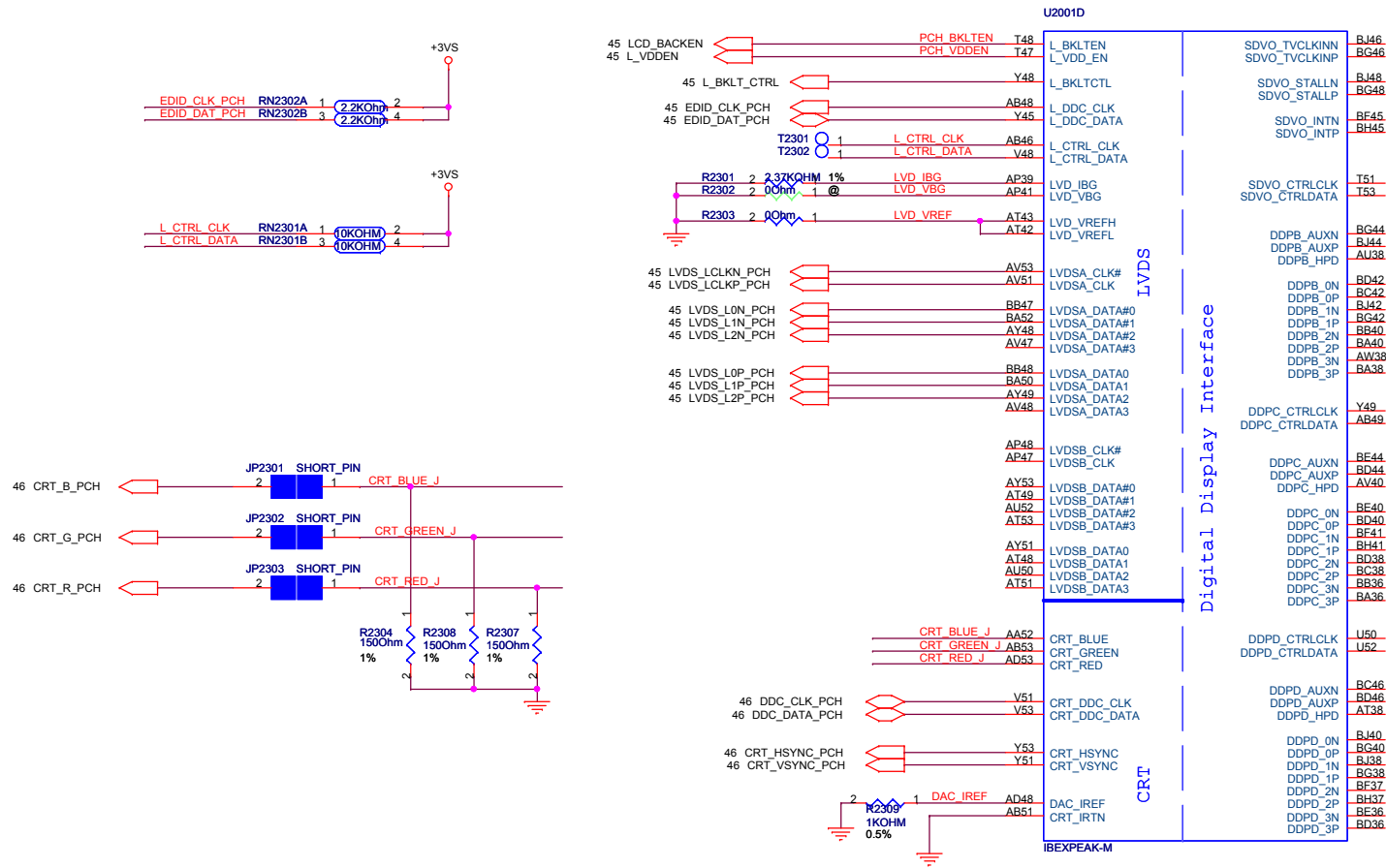
SPI MOSI: iTPM strap.

```
Mount R2015: Enable
Unmount R2015: Disable(default)
```





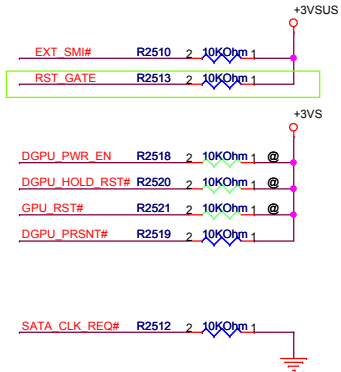








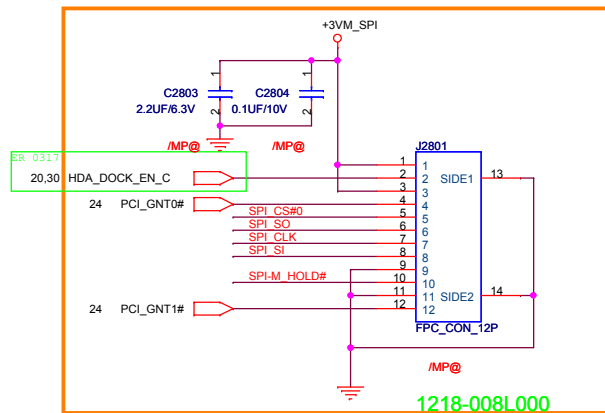
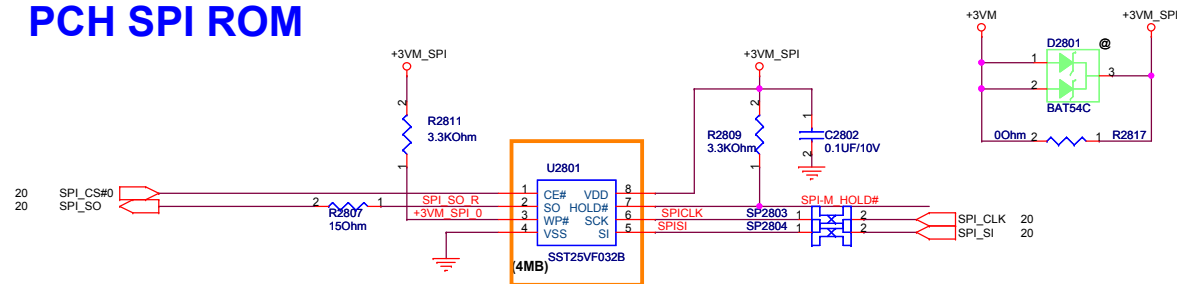
GPIO 27:Enable VCCVRM,Low=disable.  
Default internal pull up.



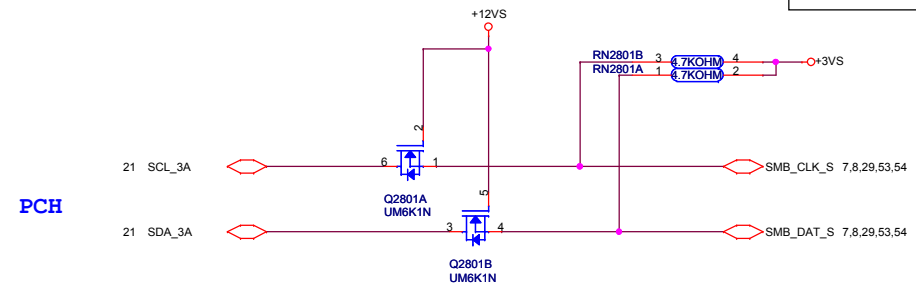




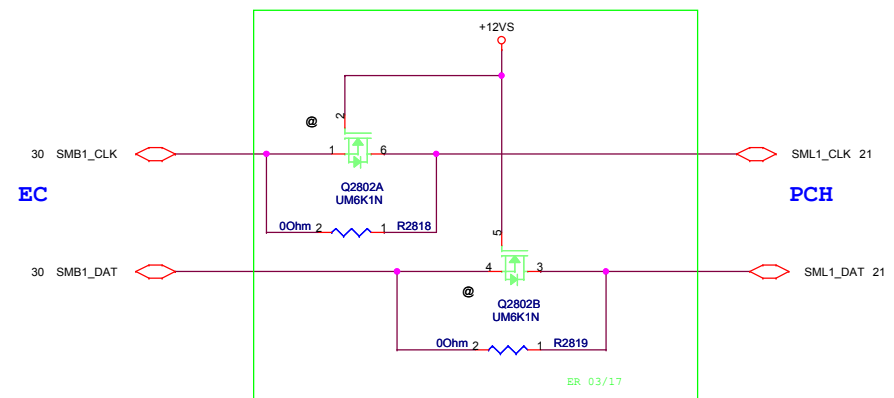
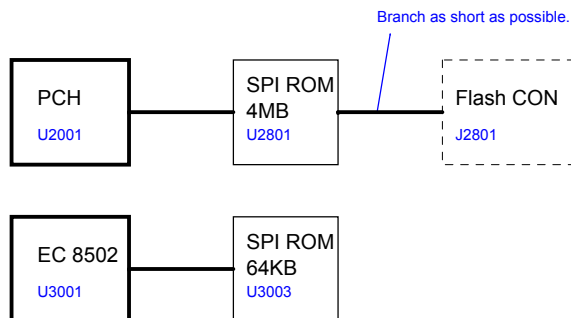
# PCH SPI ROM

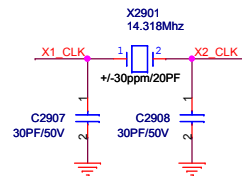
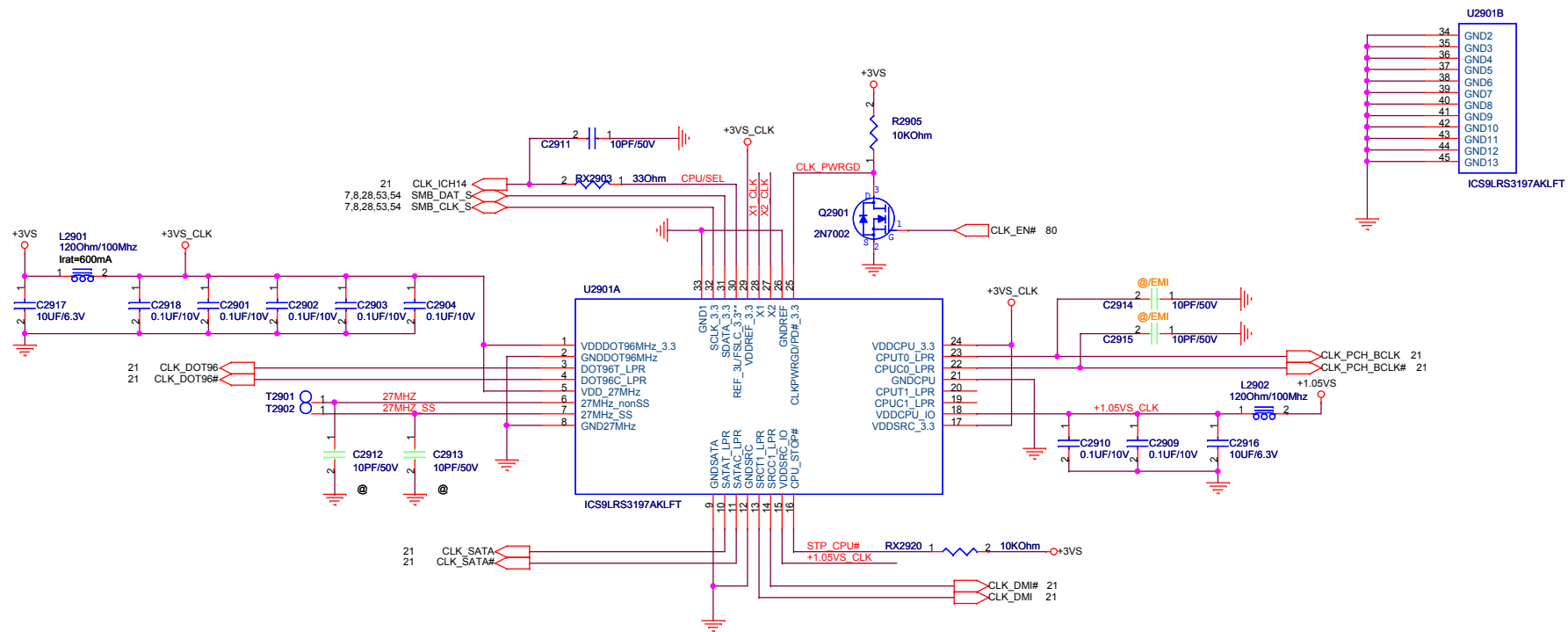


**SMBUS Link device**  
DDR  
CLKGEN  
DEBUG  
WLAN

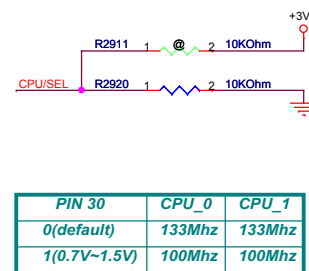


## SPI Setting for layout:





Pin30 CPU select :

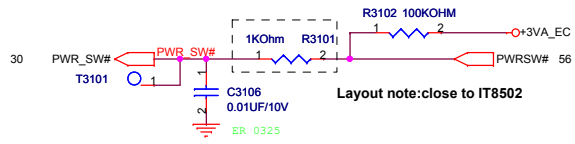




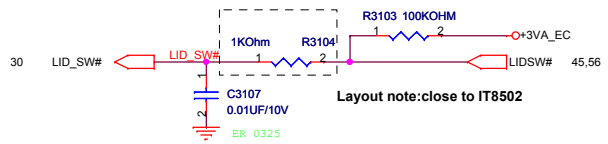


For Switch

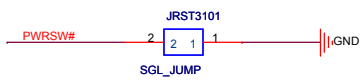
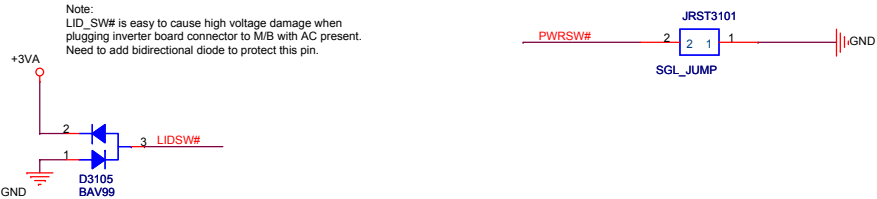
PWR SWITCH



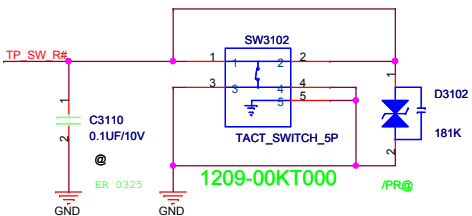
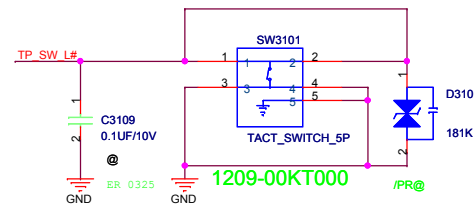
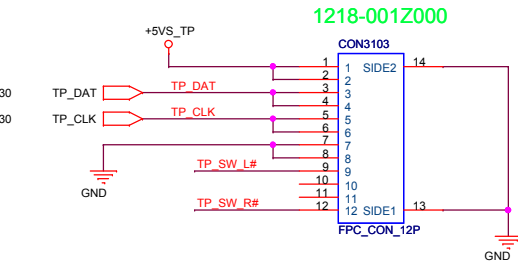
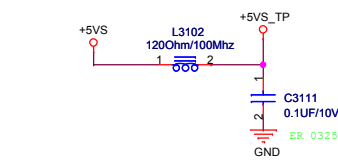
LID SWITCH



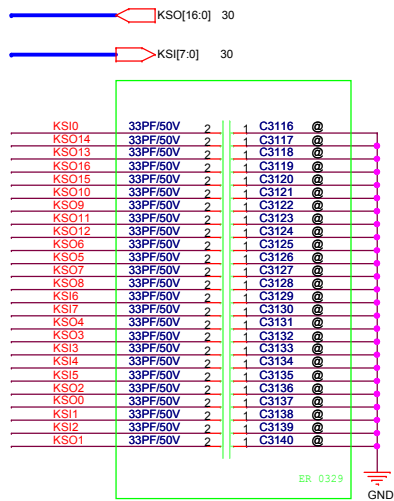
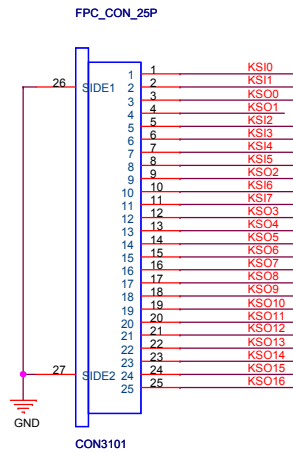
Note:  
LID\_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.



Touch-Pad



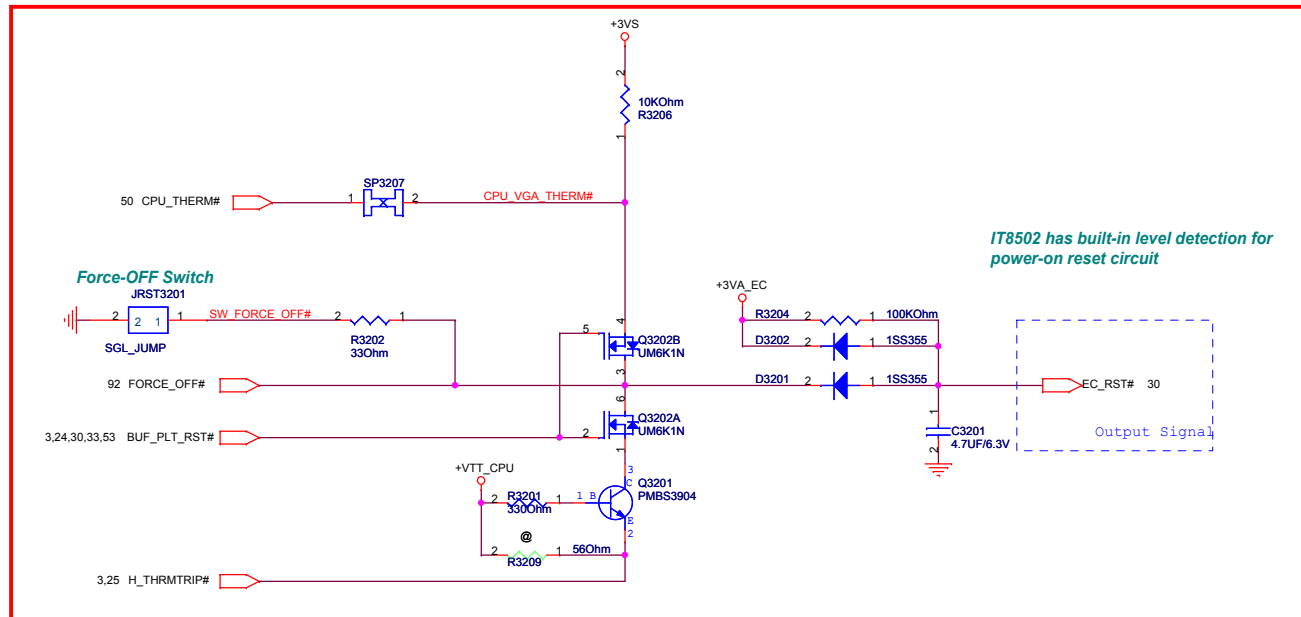
Keyboard Connector

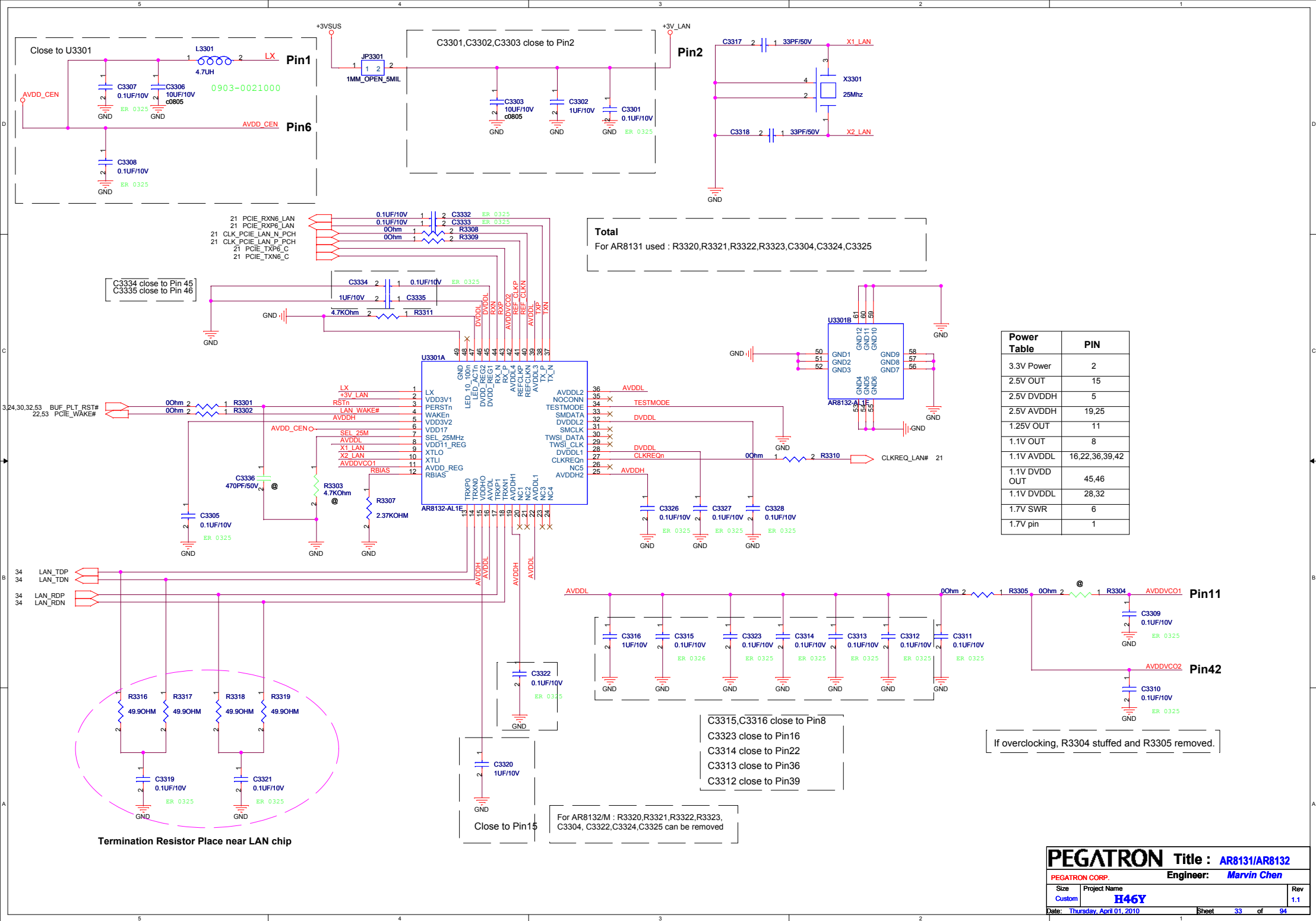


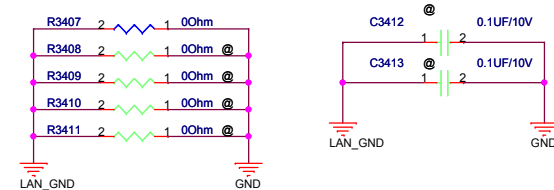
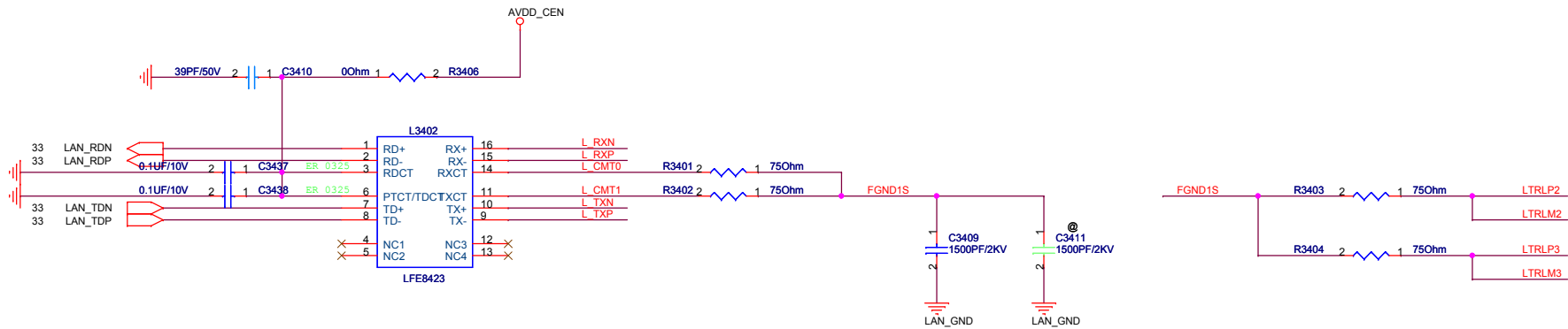
1218-001Z000

1218-0009000

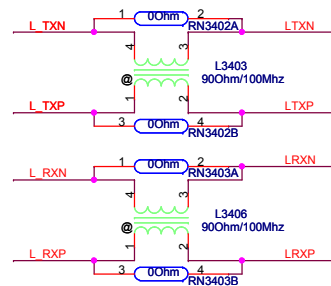
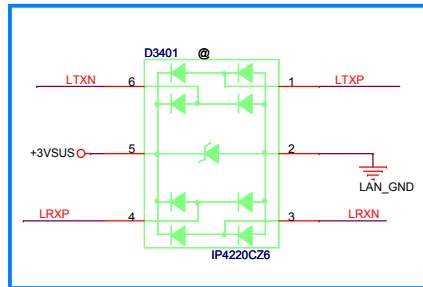
## Thermal Policy



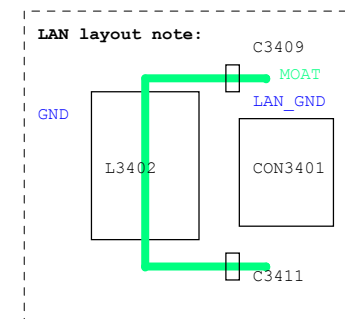
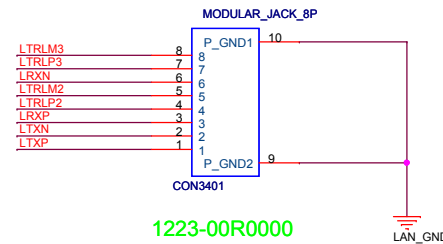




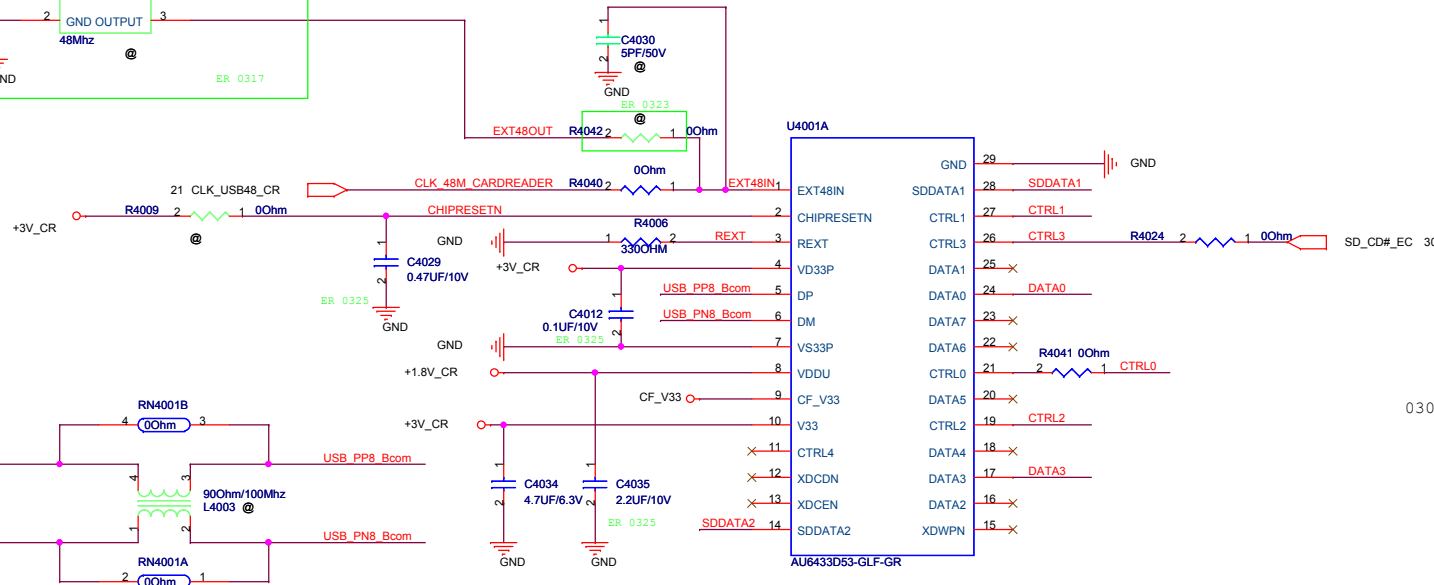
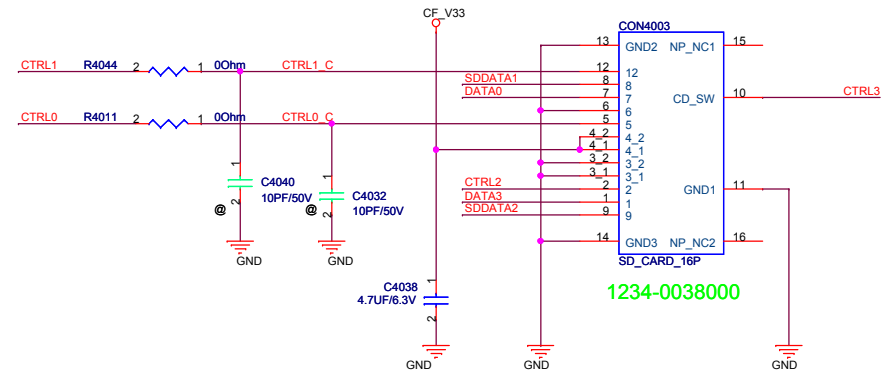
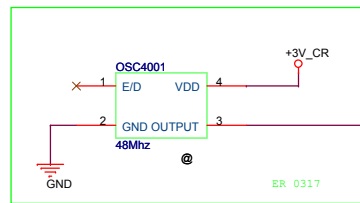
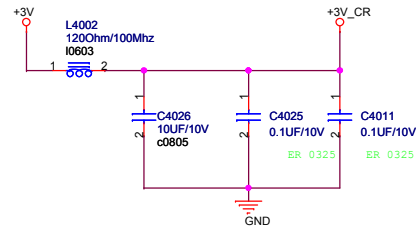
FOR EMI  
Co-Layout



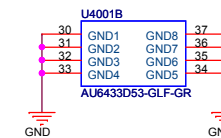
RJ45

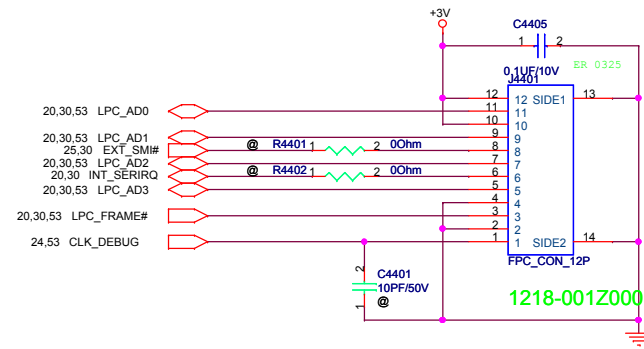


# CARD READER CONNECTOR

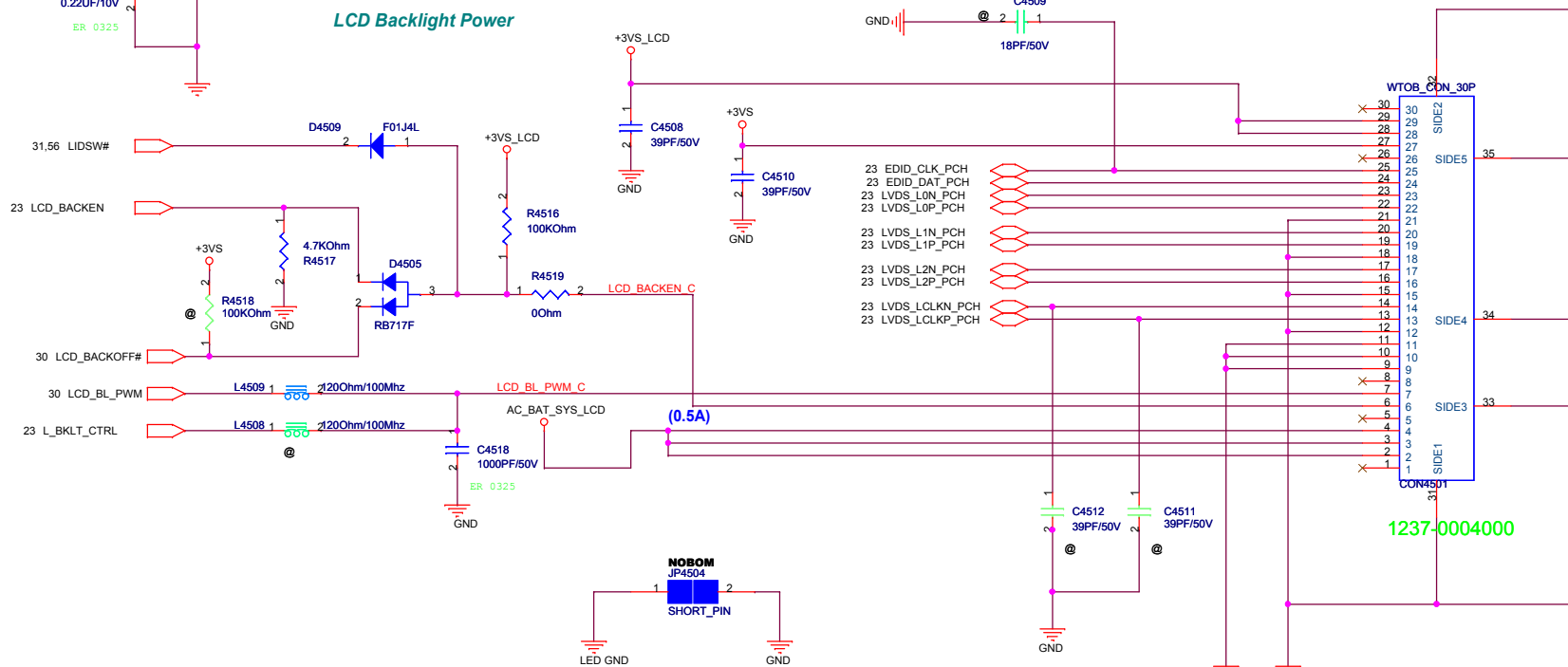
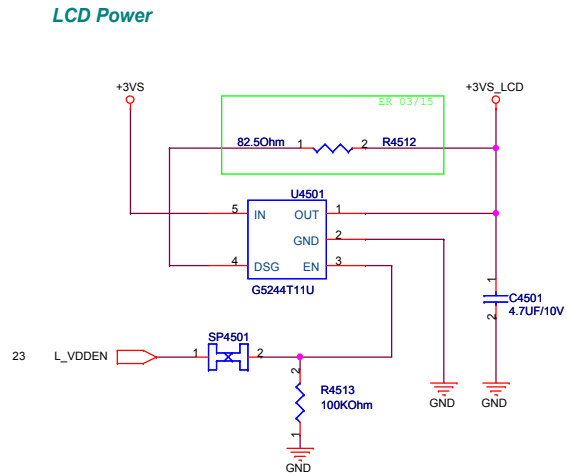
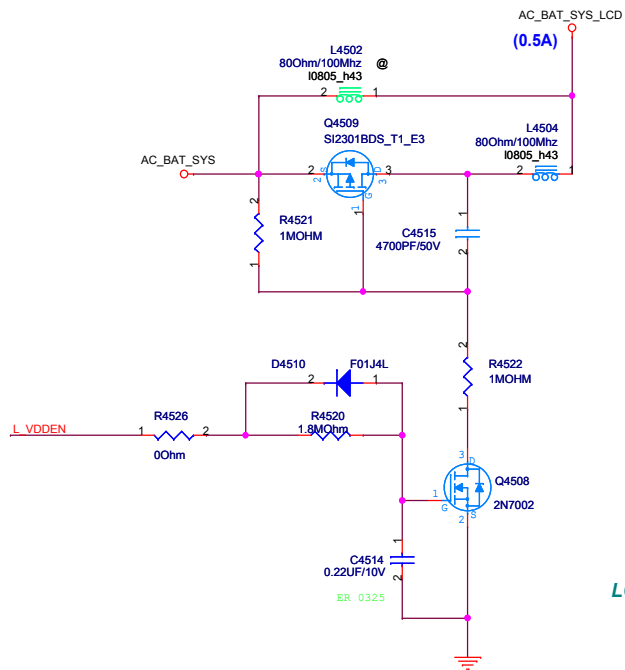


0304 for card reader chip via

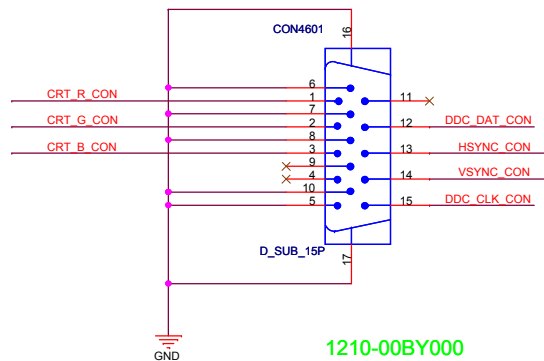




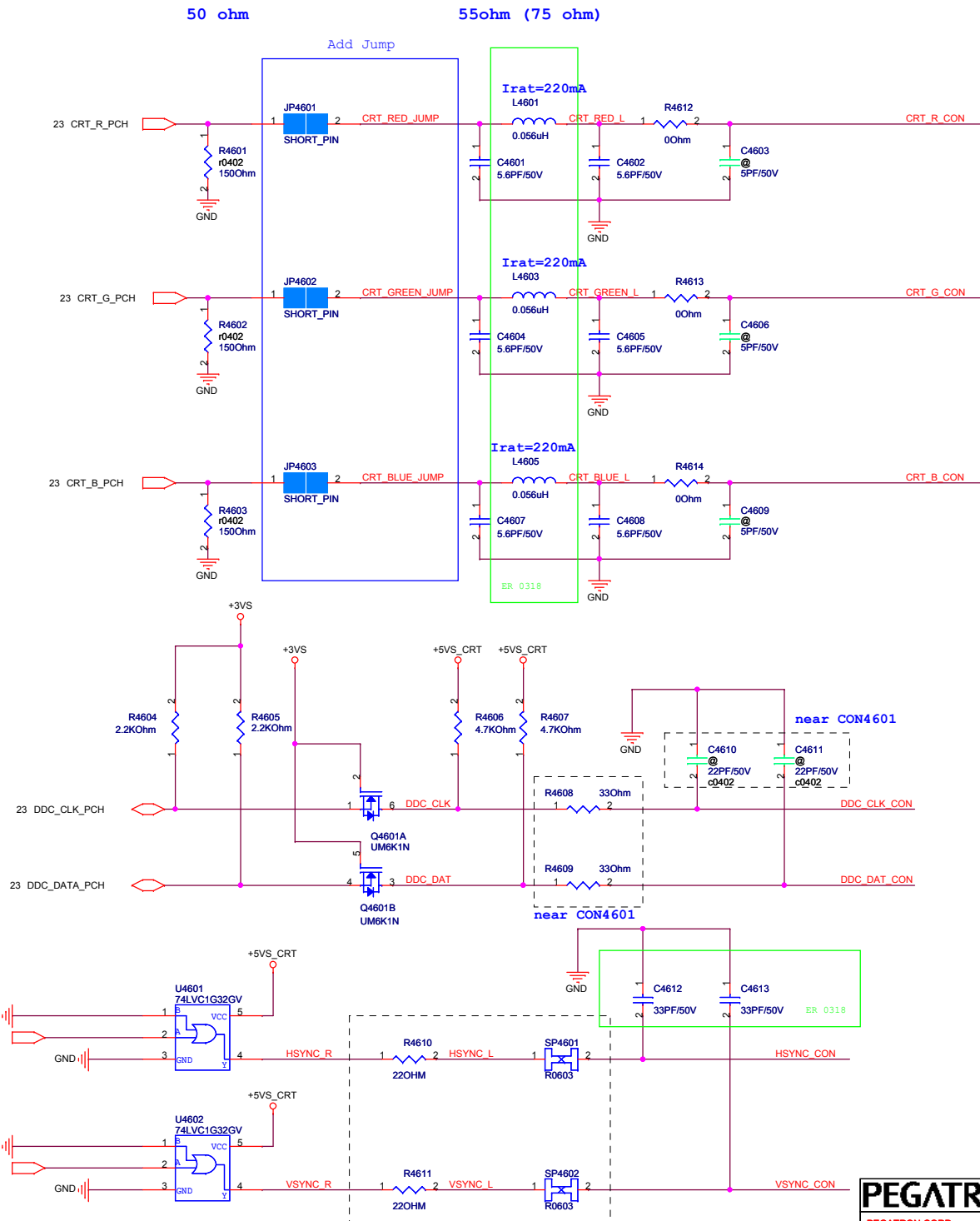
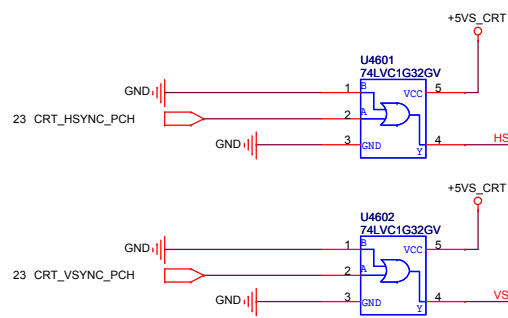
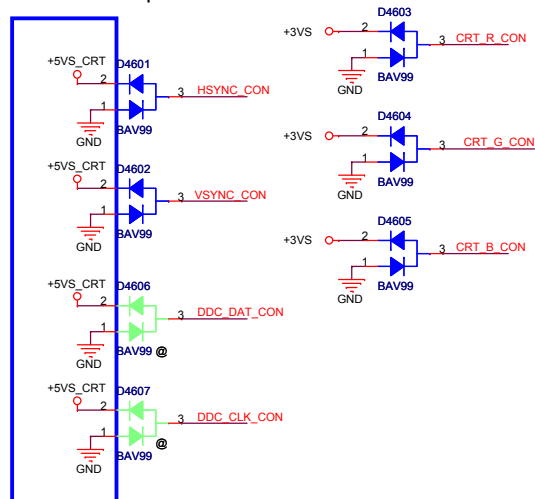


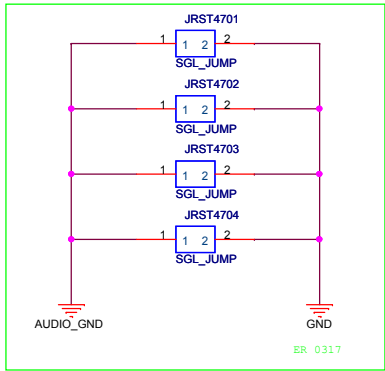


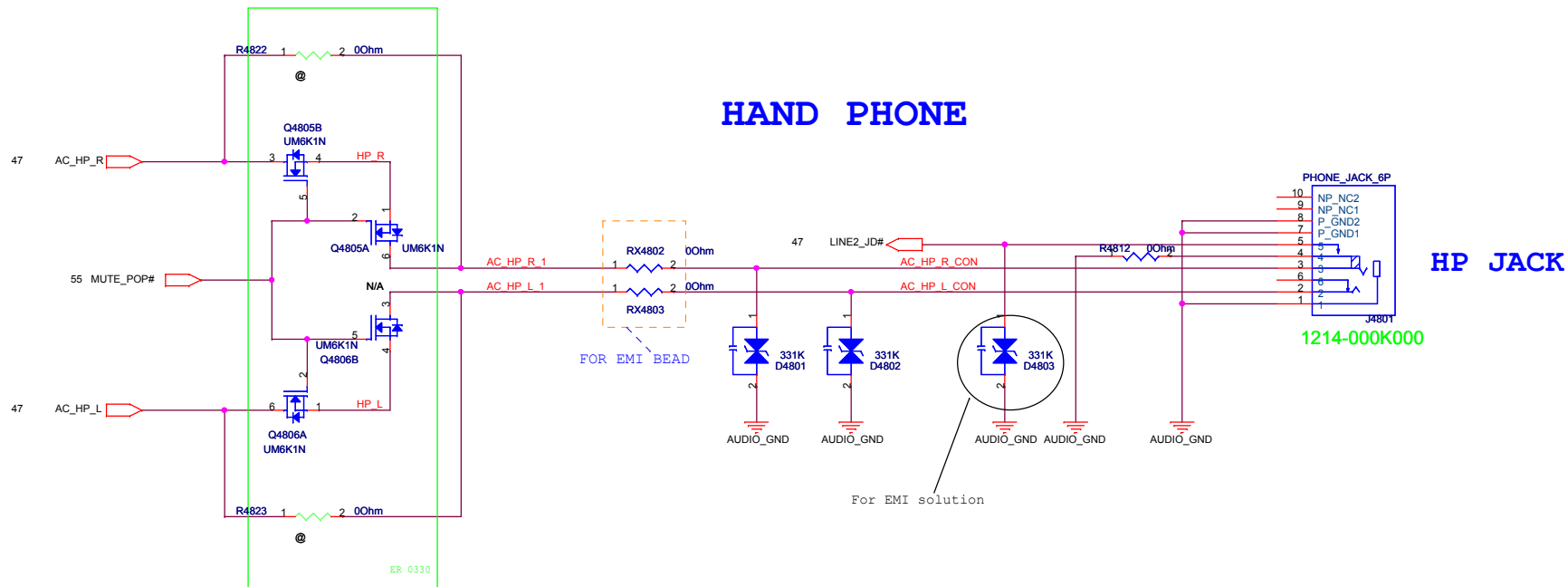
**LED Power Supply 7V~20V**



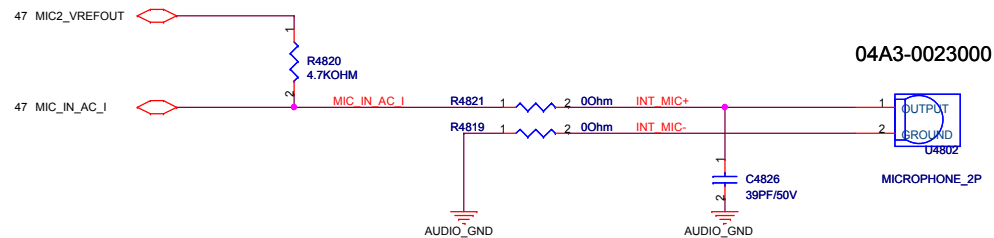
PLACE ESD Diodes near  
VGA port

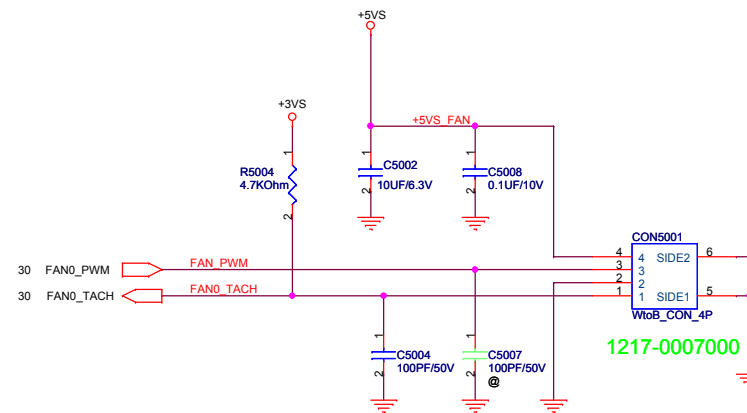
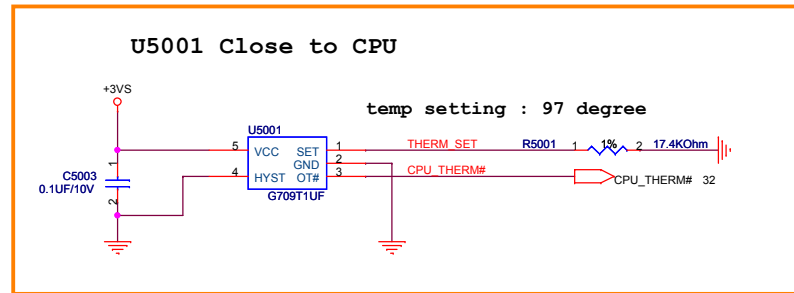


$$V_{out} = 1.25 * (1 + (100K / 34.8K)) = 4.84V$$


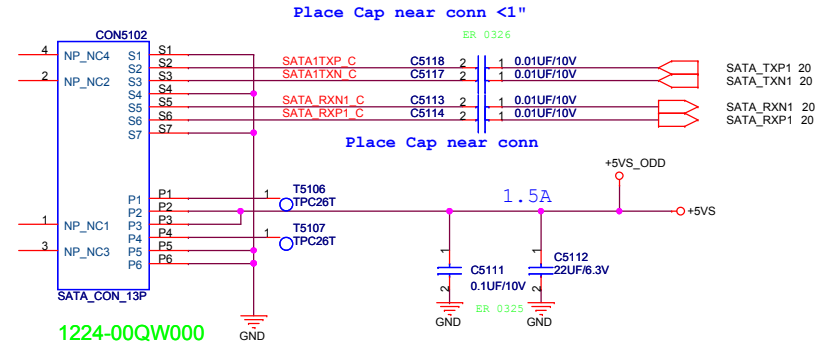
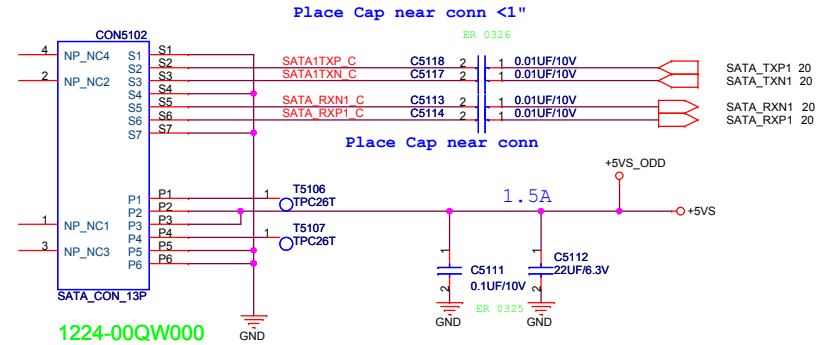


## INTERNAL MICROPHONE (Analog MIC)

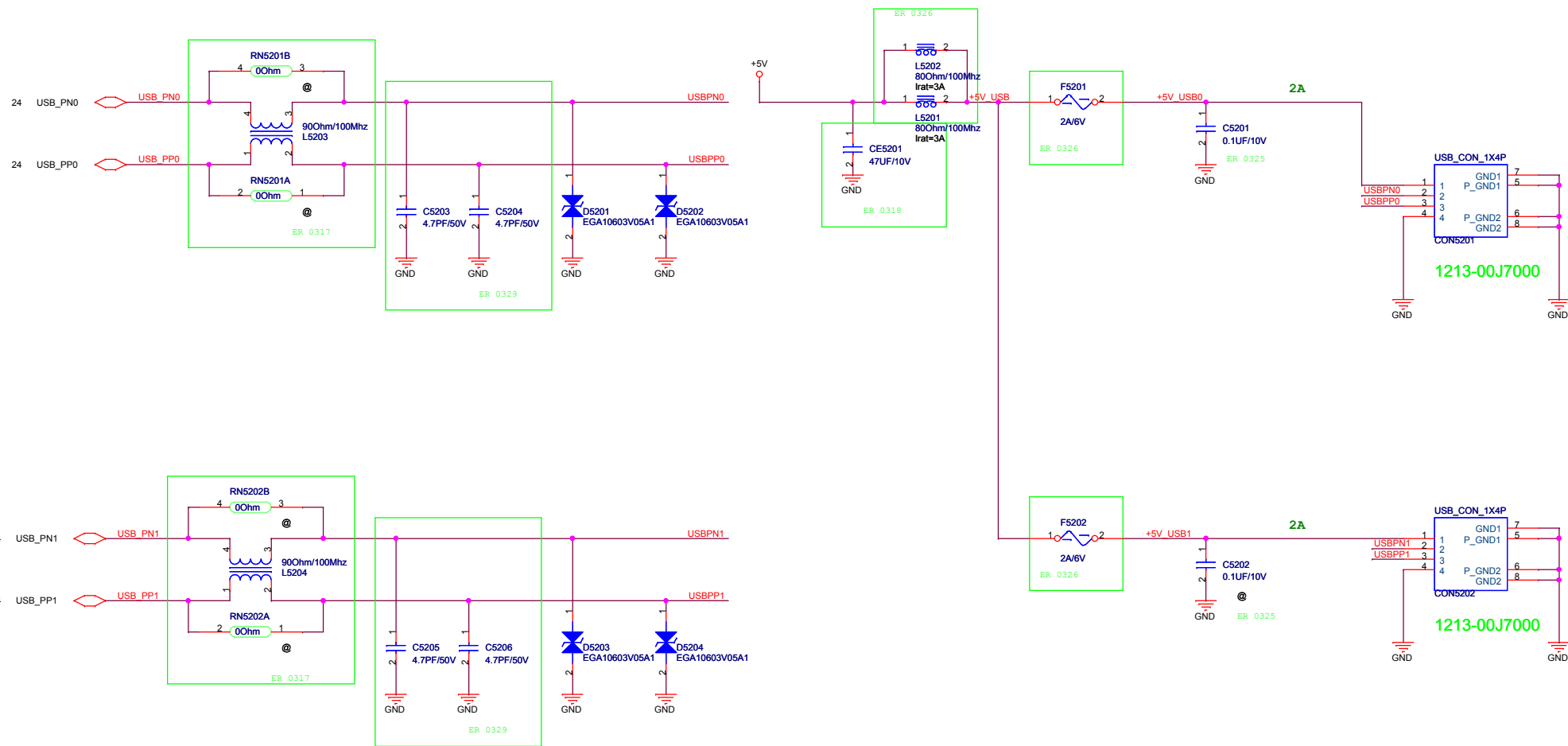


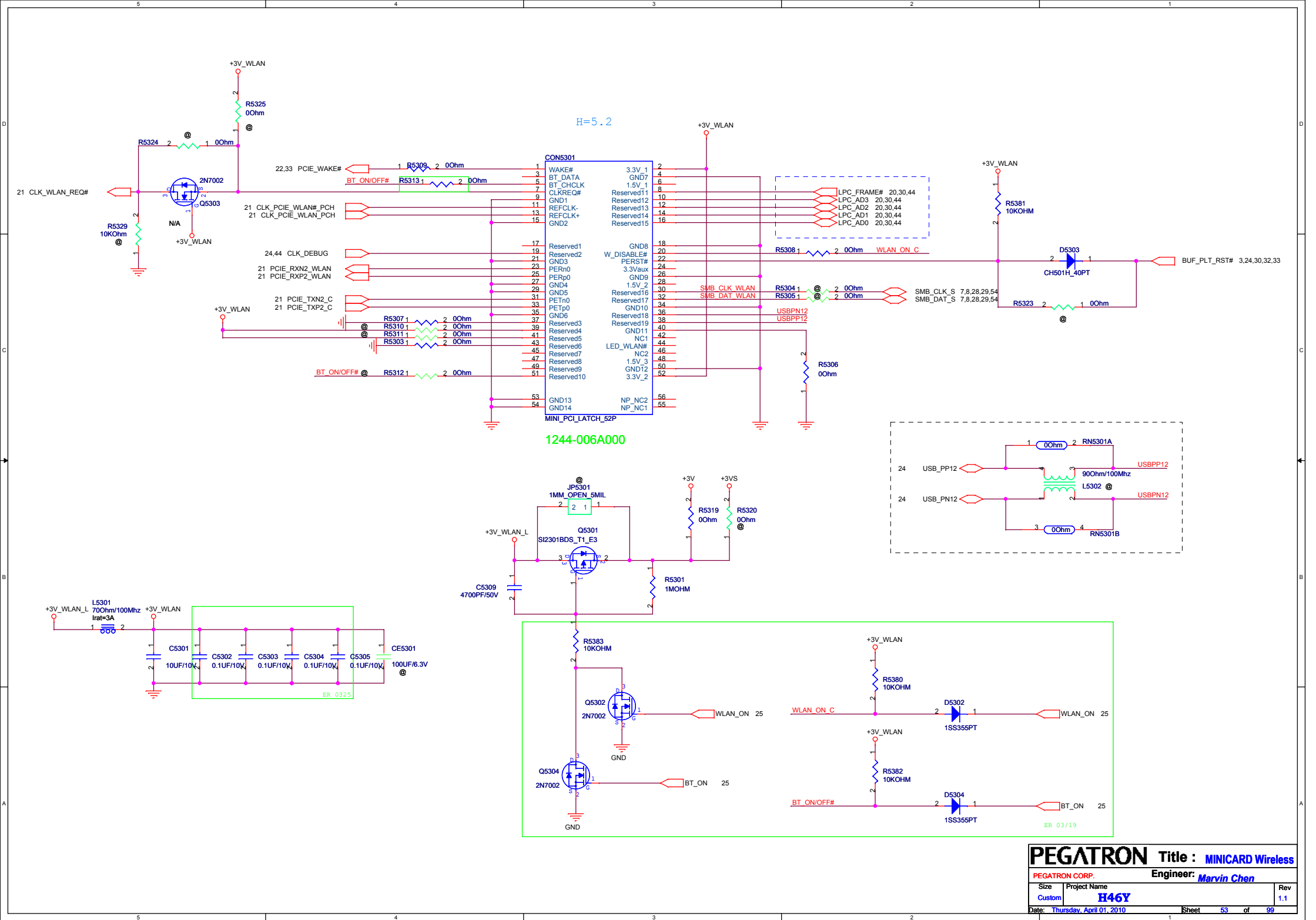


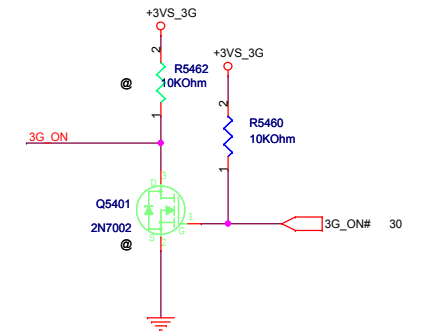
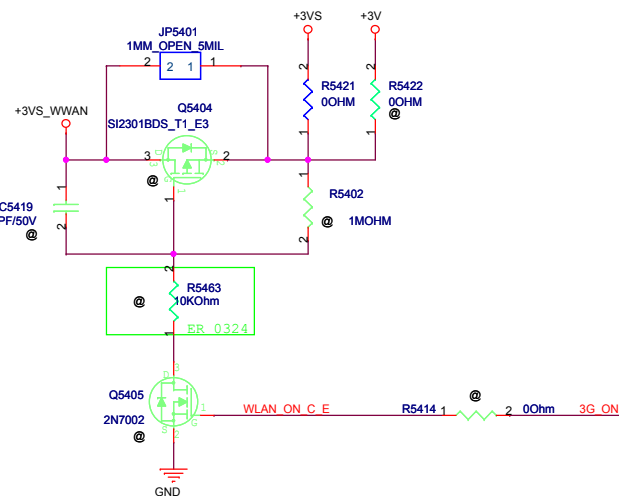
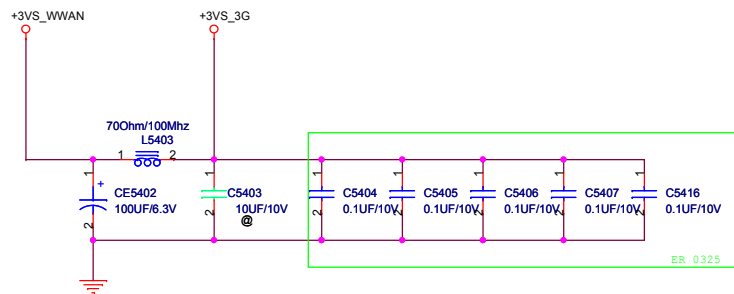
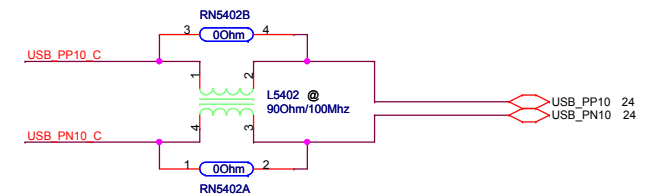
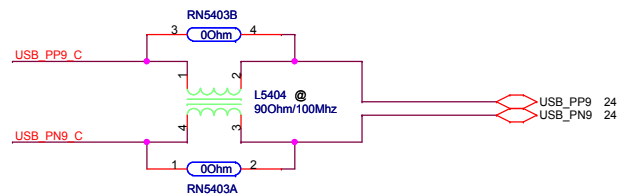
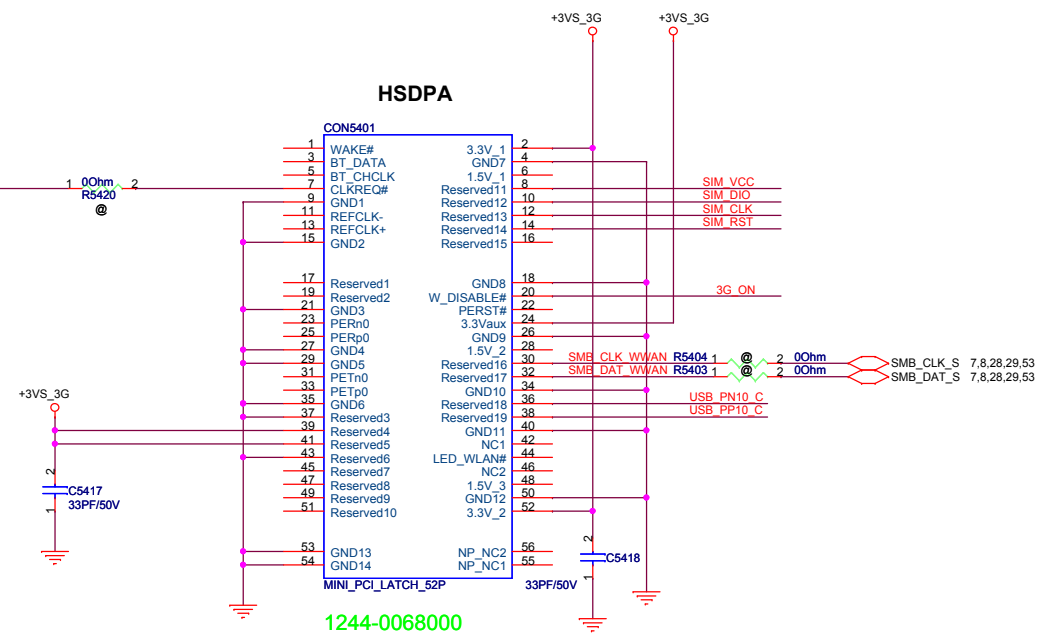
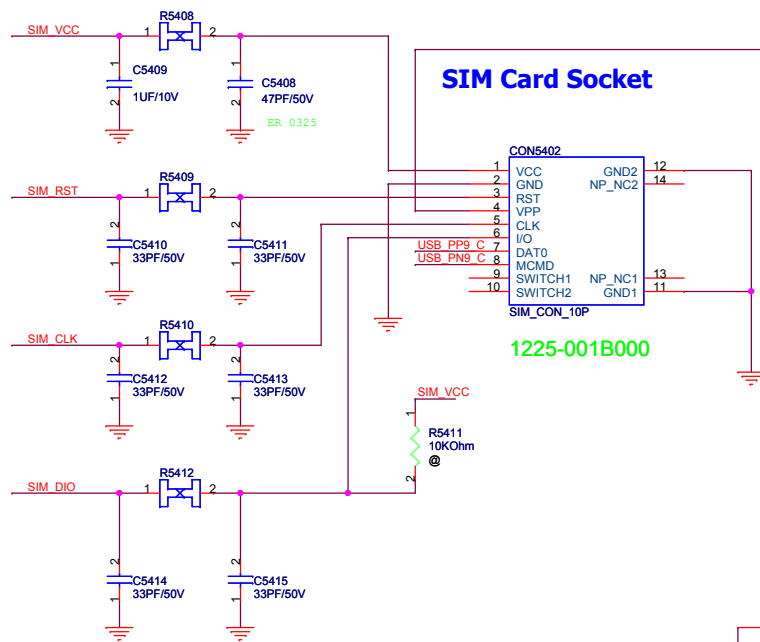
## SATA ODD

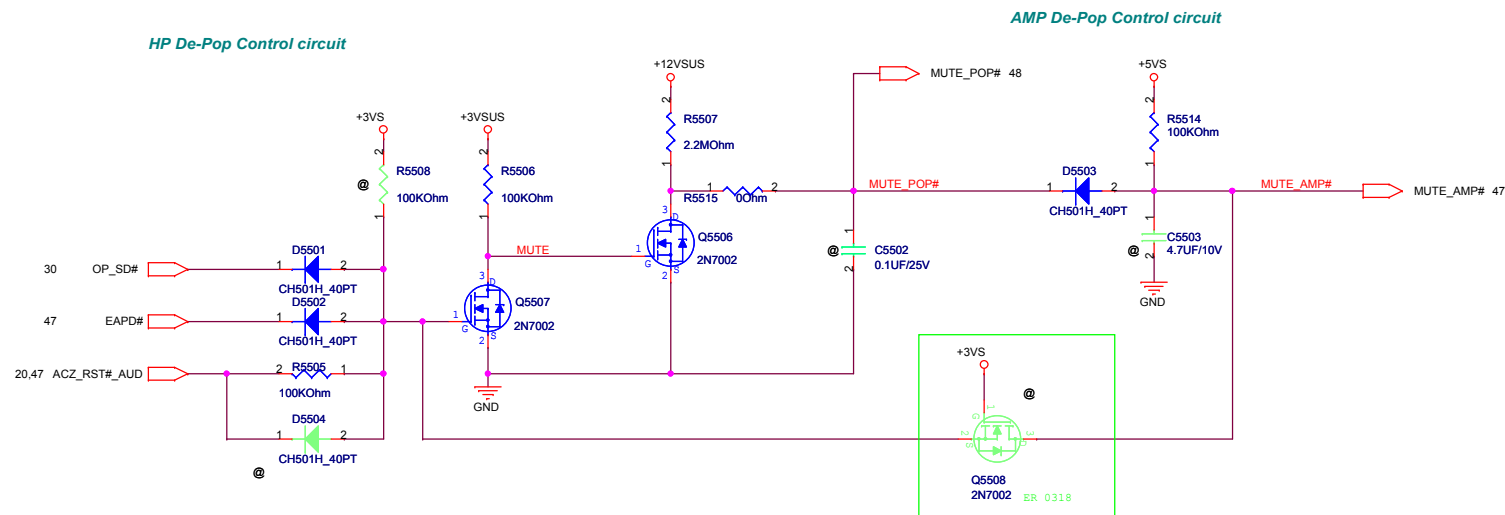




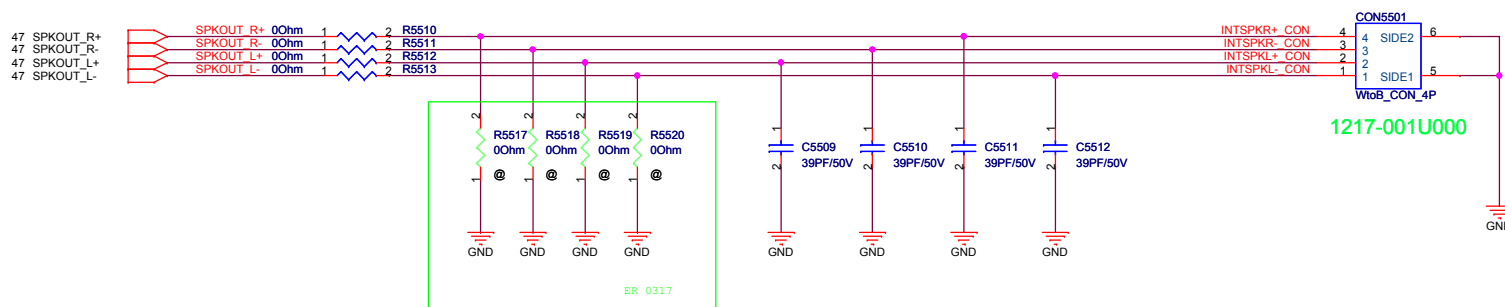




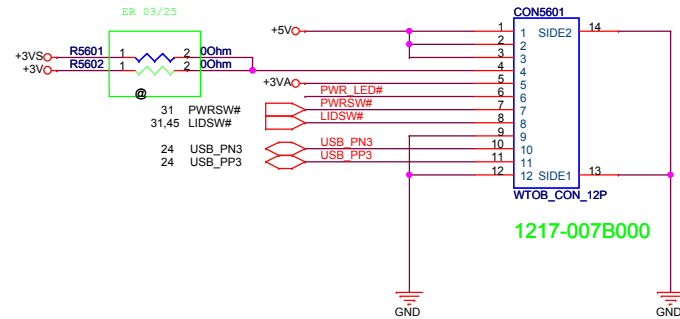




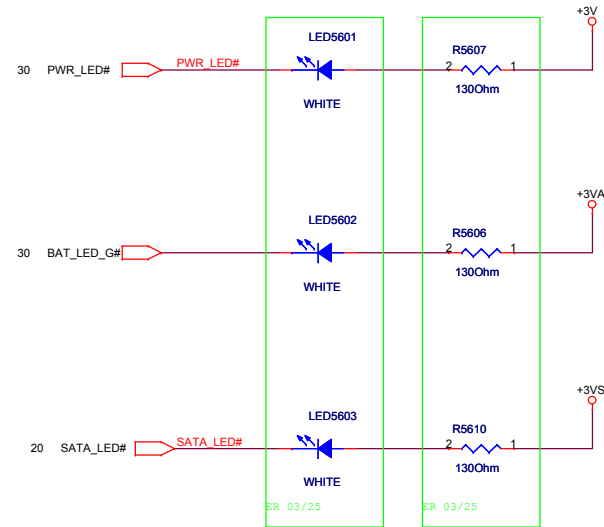
## SPEAKER CONNECTOR (1.5W)

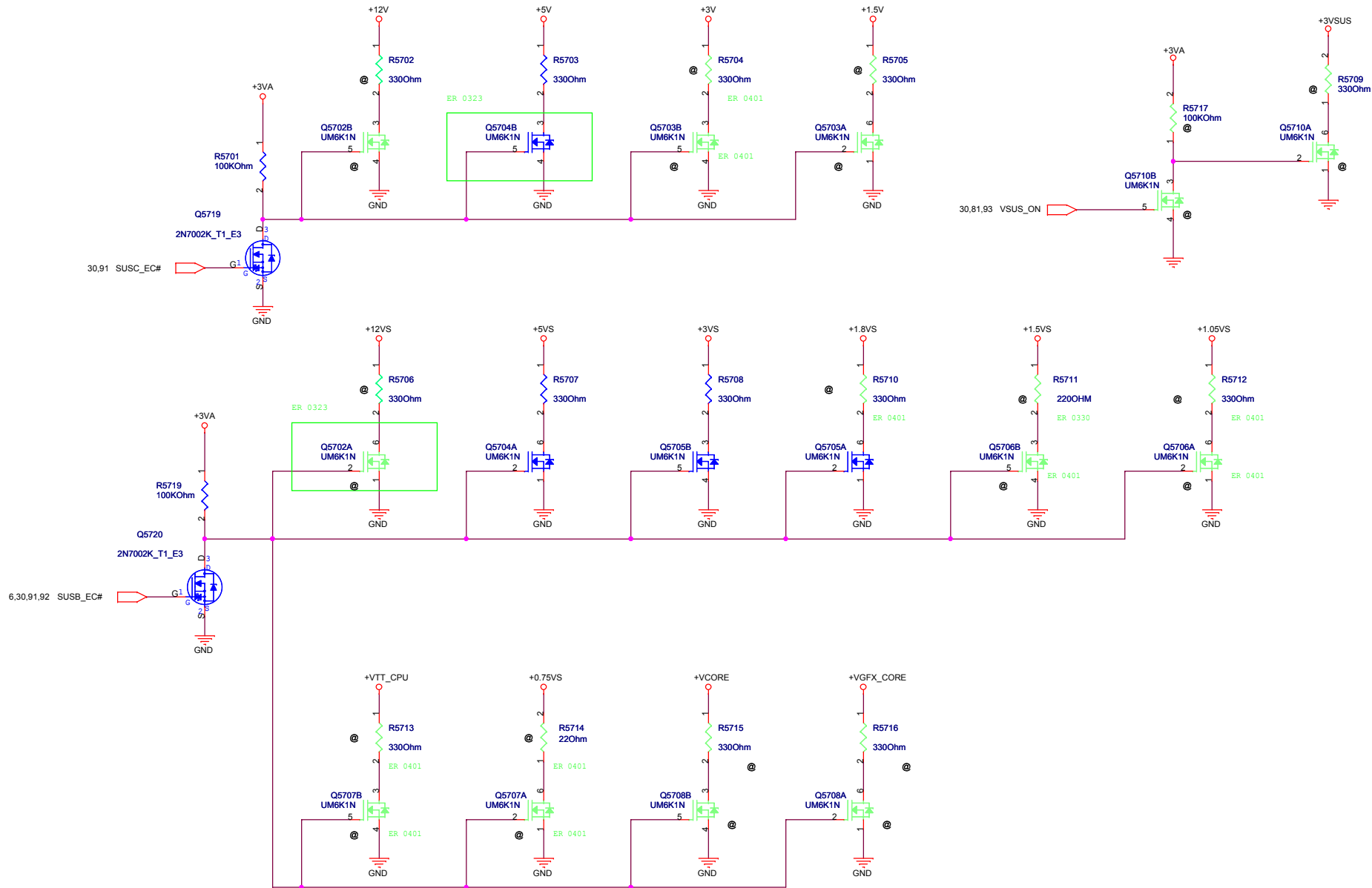


## Power SW CONN.

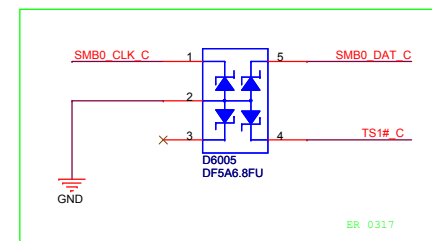
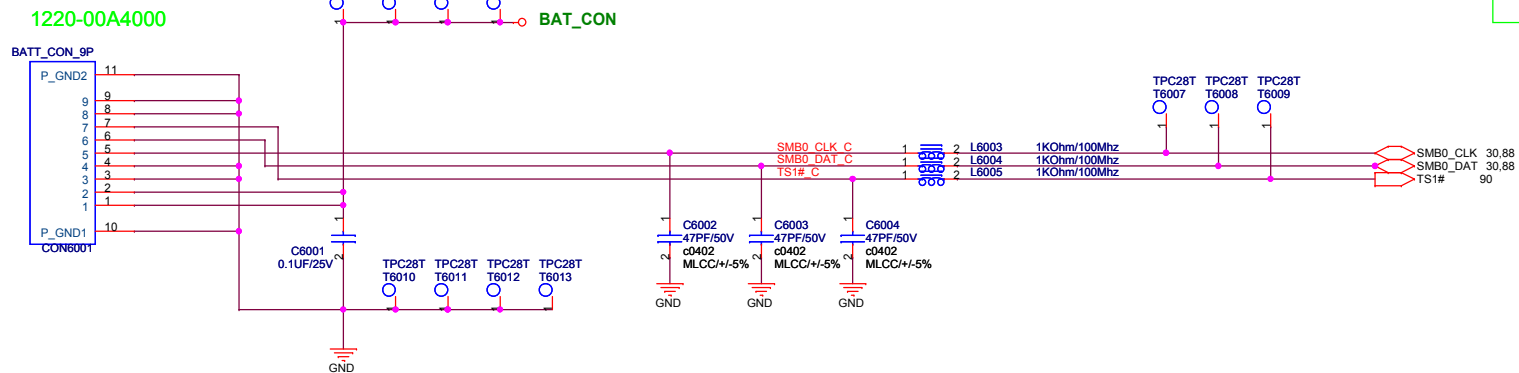


## LED



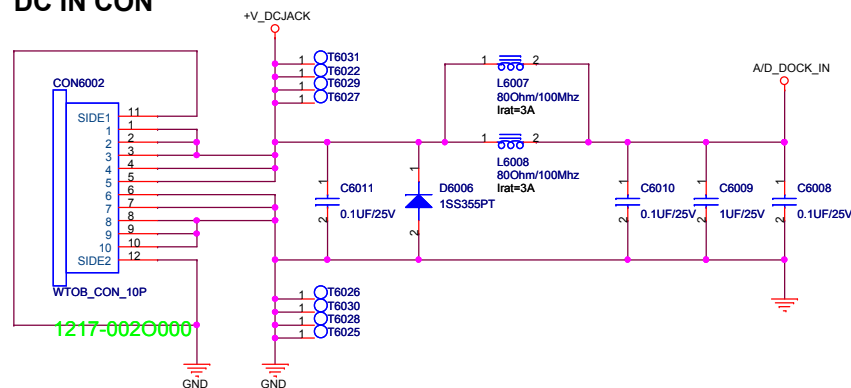


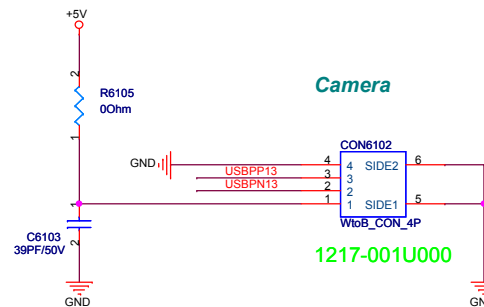
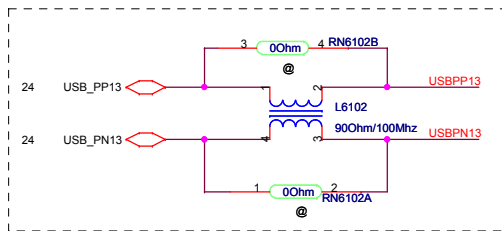
# BATTERY



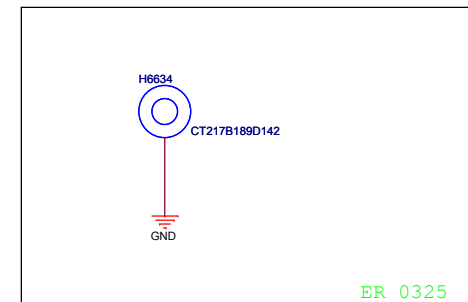
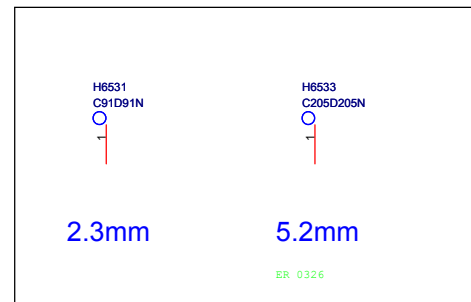
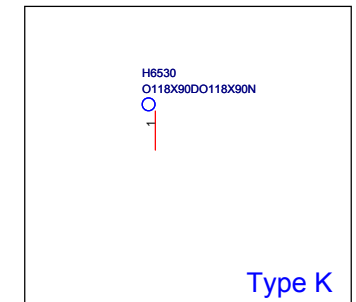
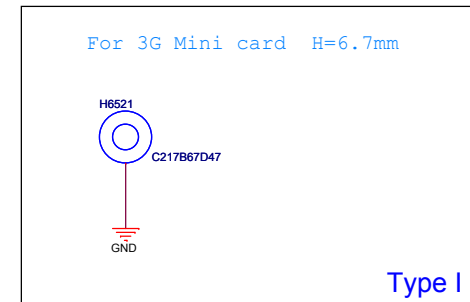
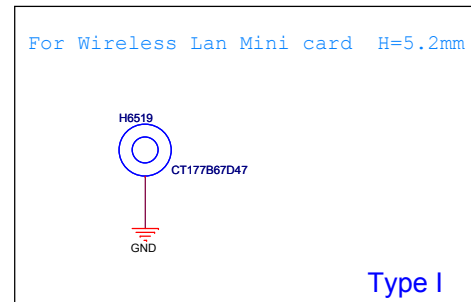
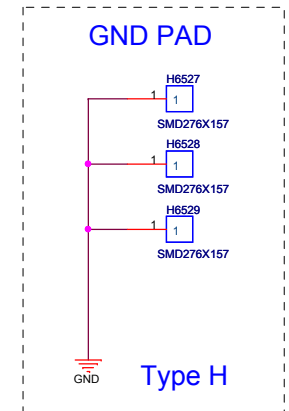
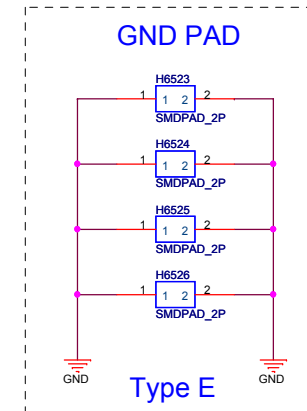
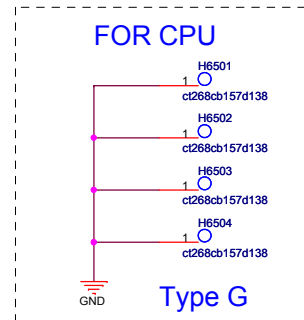
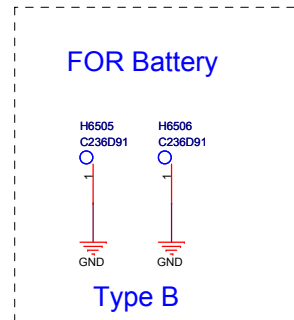
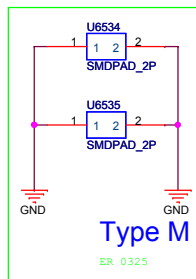
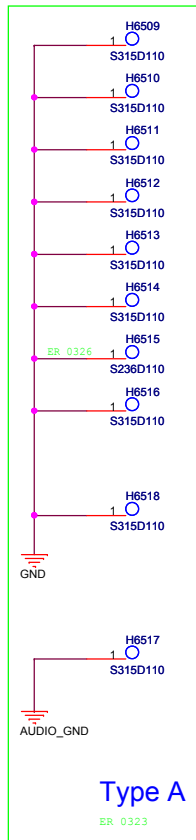
# DC JACK-IN

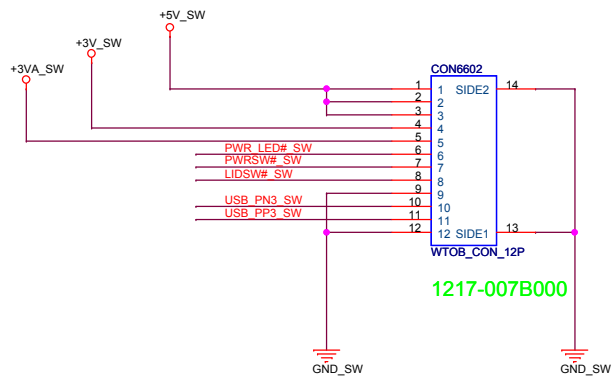
## DC IN CON



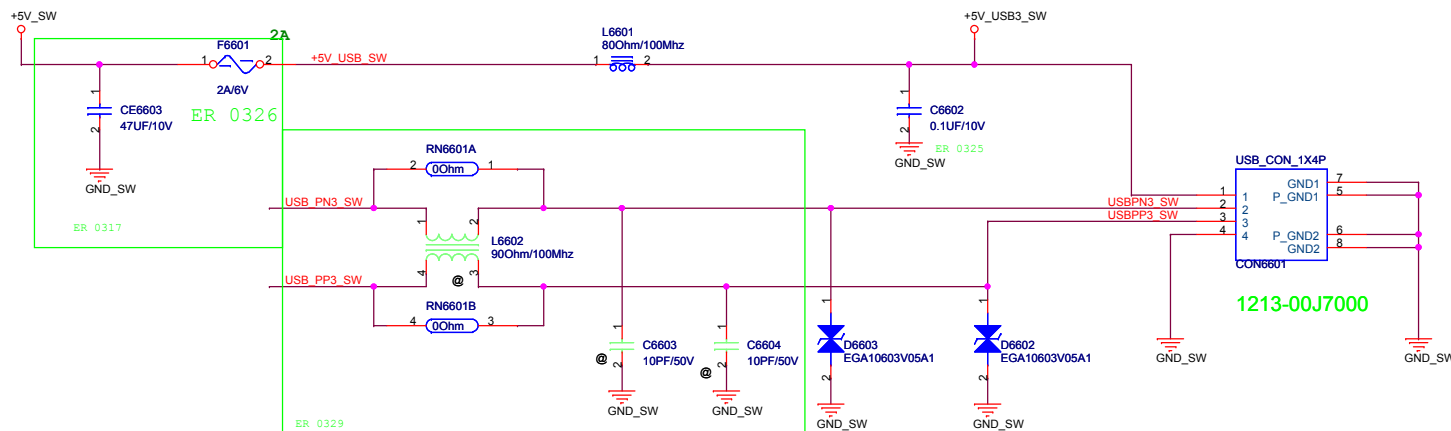
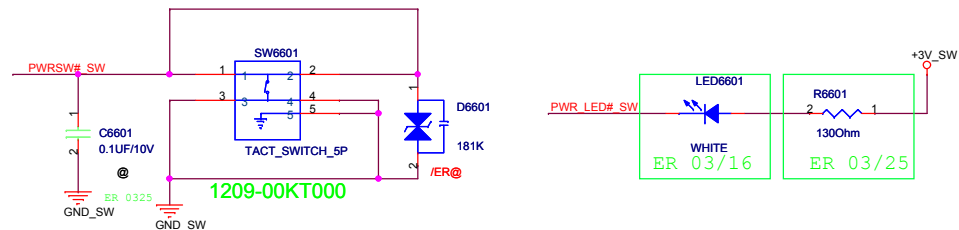




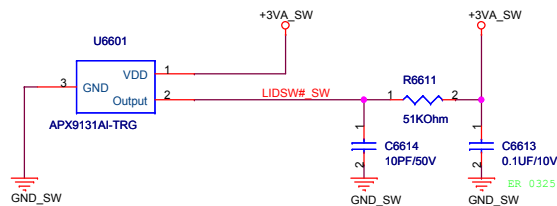




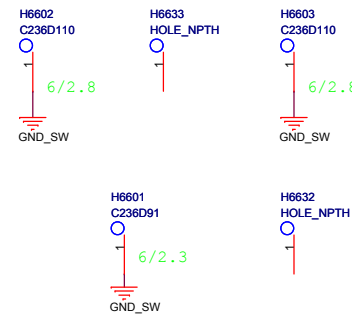
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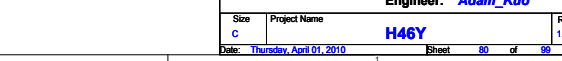
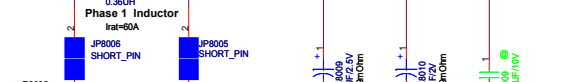
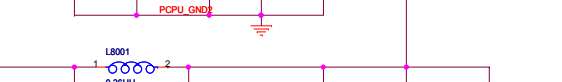
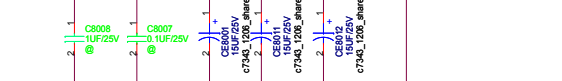
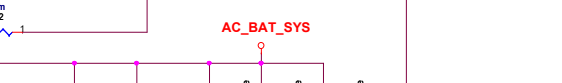
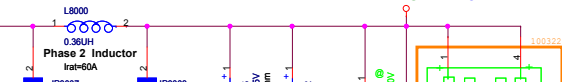
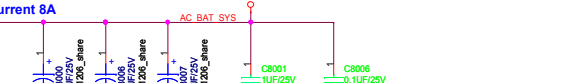
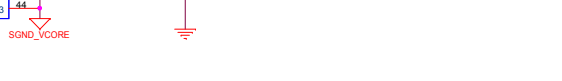
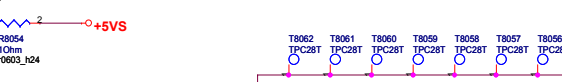
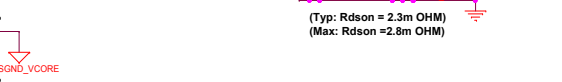
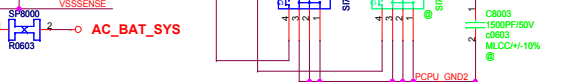
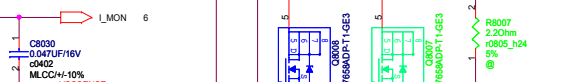
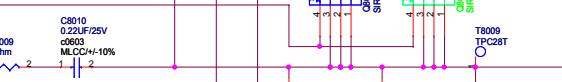
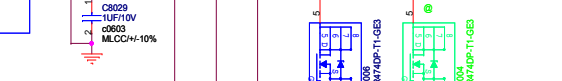
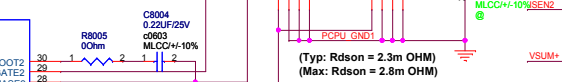
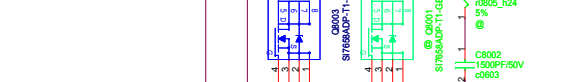
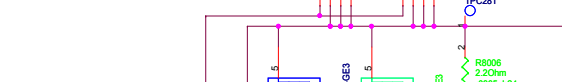
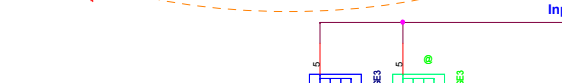
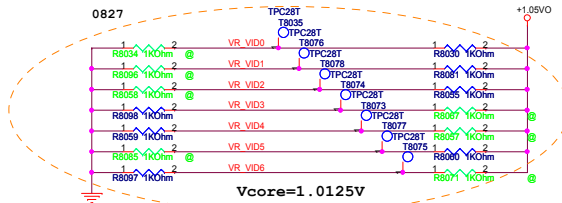
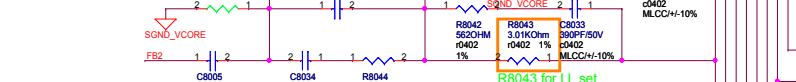
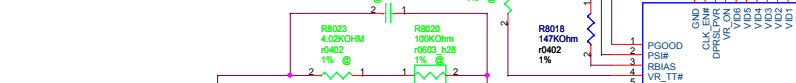
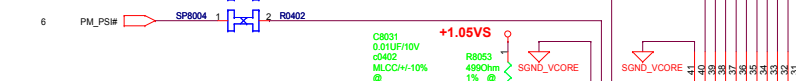
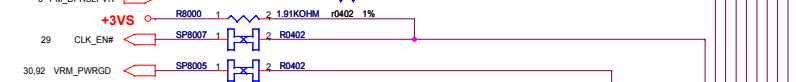
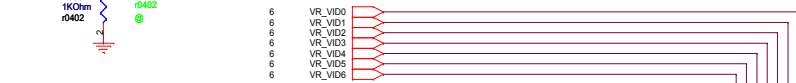
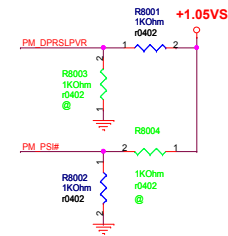


## LID SWITCH



## Screw Hole



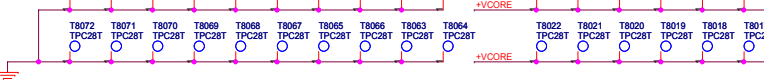
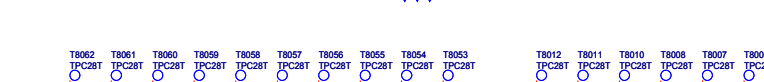
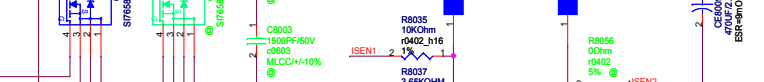
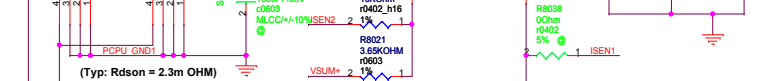
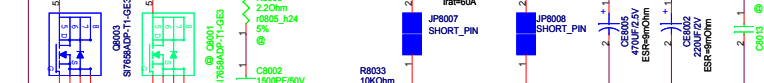
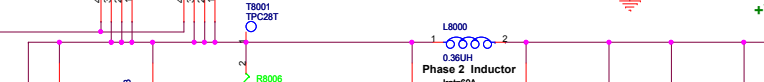
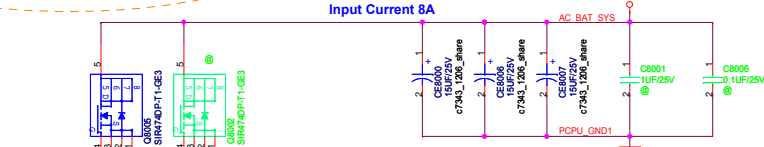


R8024=(Period(us)-0.29)\*2.65  
Period(us)=1/300KHz  
Adjust R8043 for  
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

| PM_DPRS_LV | PM_PS# | VO_action   |
|------------|--------|-------------|
| L          | L      | 1 Phase DE  |
| H          | L      | 1 Phase DE  |
| L          | H      | 2 Phase CCM |
| H          | H      | 1 Phase DE  |

R8048 for OCP set



AC\_BAT\_SYS

+Vcore 48A

AC\_BAT\_SYS

AC\_BAT\_SYS

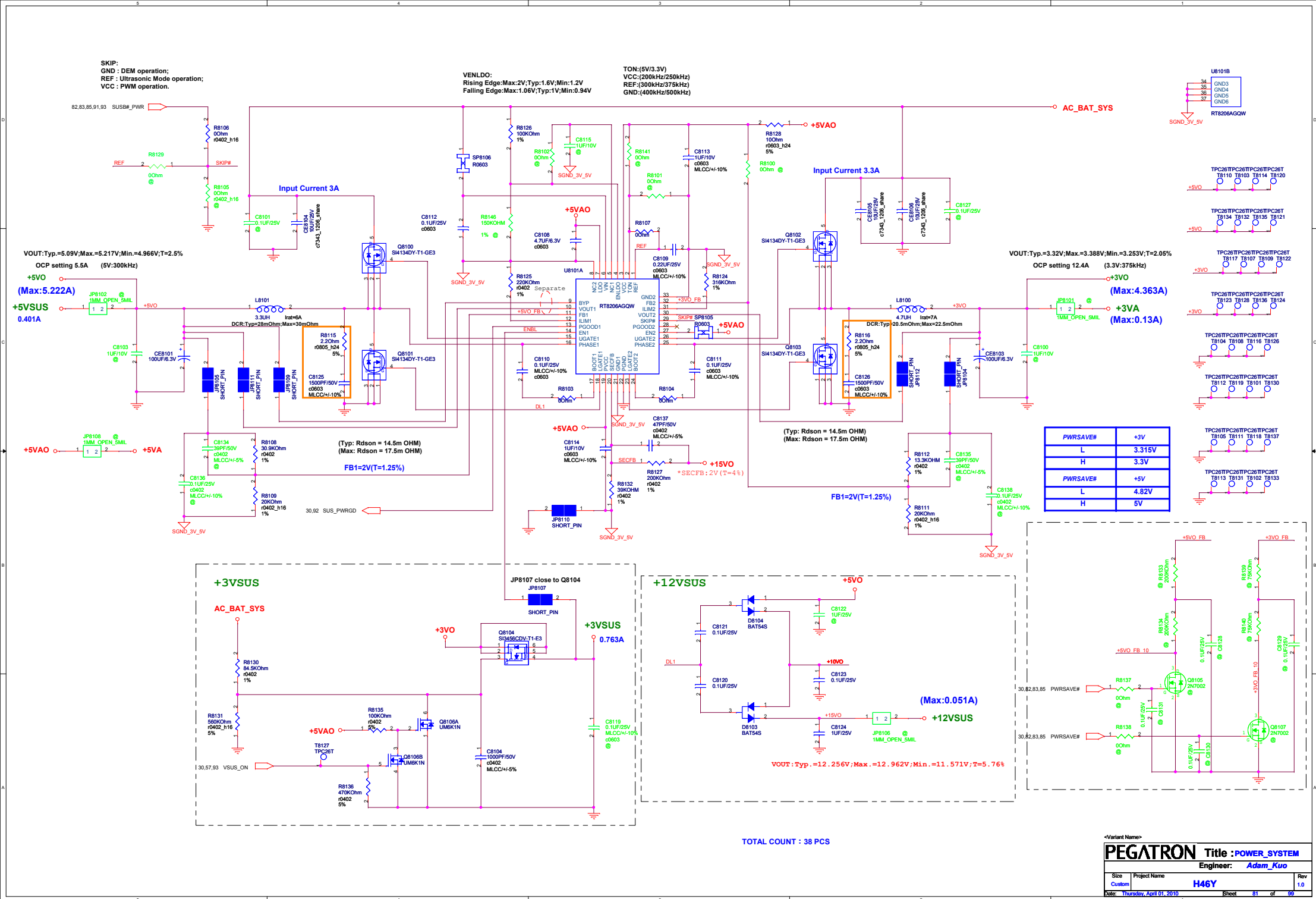
AC\_BAT\_SYS

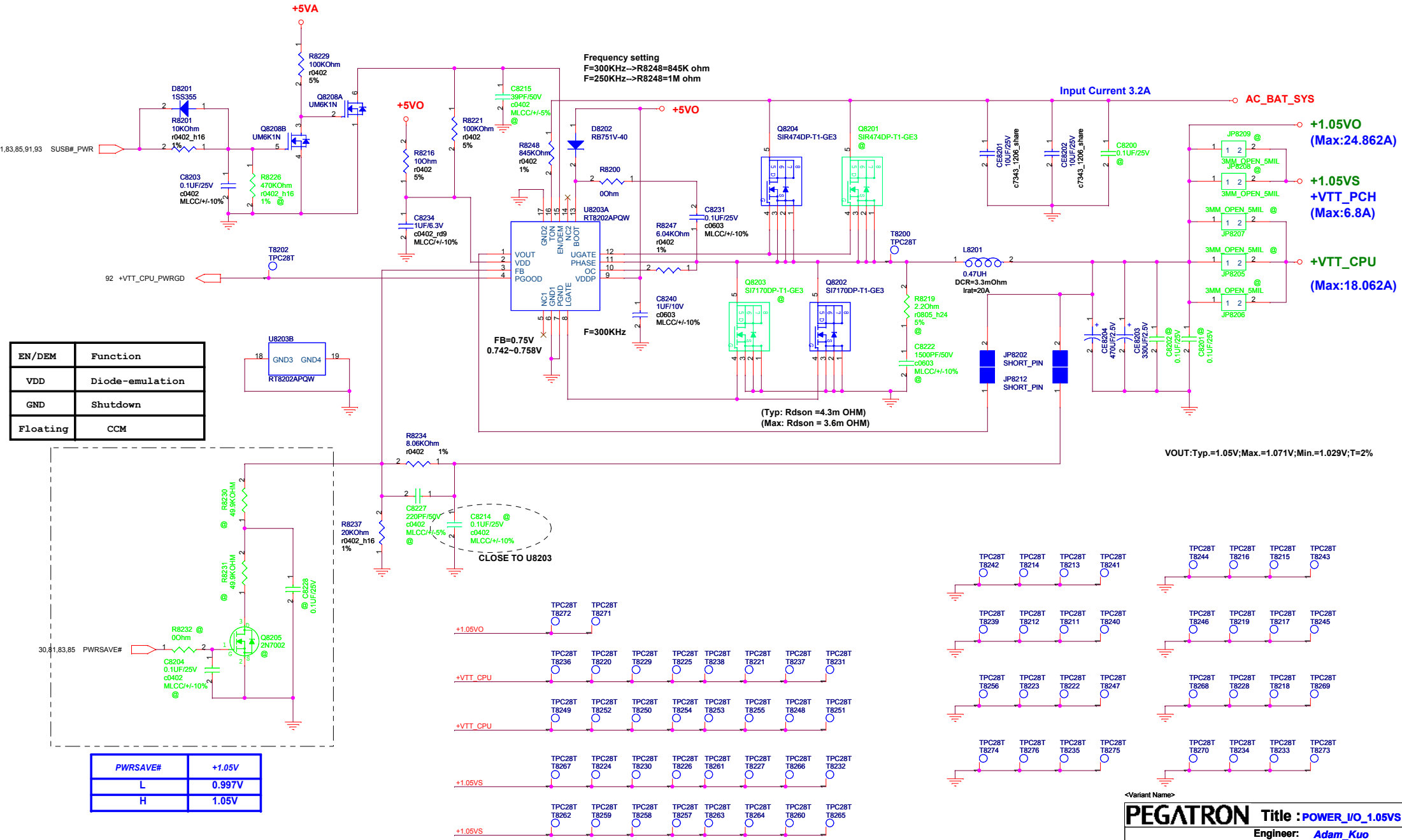
AC\_BAT\_SYS

AC\_BAT\_SYS

AC\_BAT\_SYS

AC\_BAT\_SYS



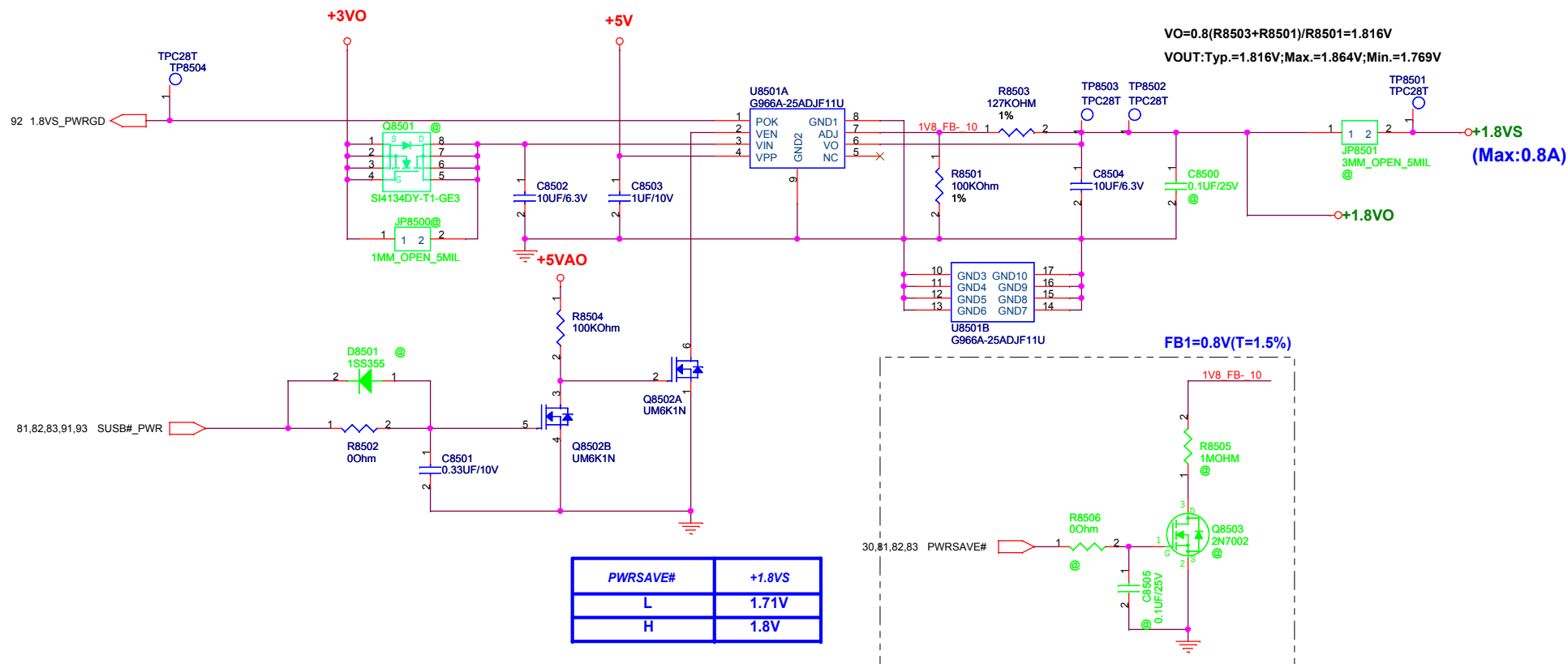


| EN/DEM   | Function        |
|----------|-----------------|
| VDD      | Diode-emulation |
| GND      | Shutdown        |
| Floating | CCM             |

| PWRSAVE# | +1.05V |
|----------|--------|
| L        | 0.997V |
| H        | 1.05V  |

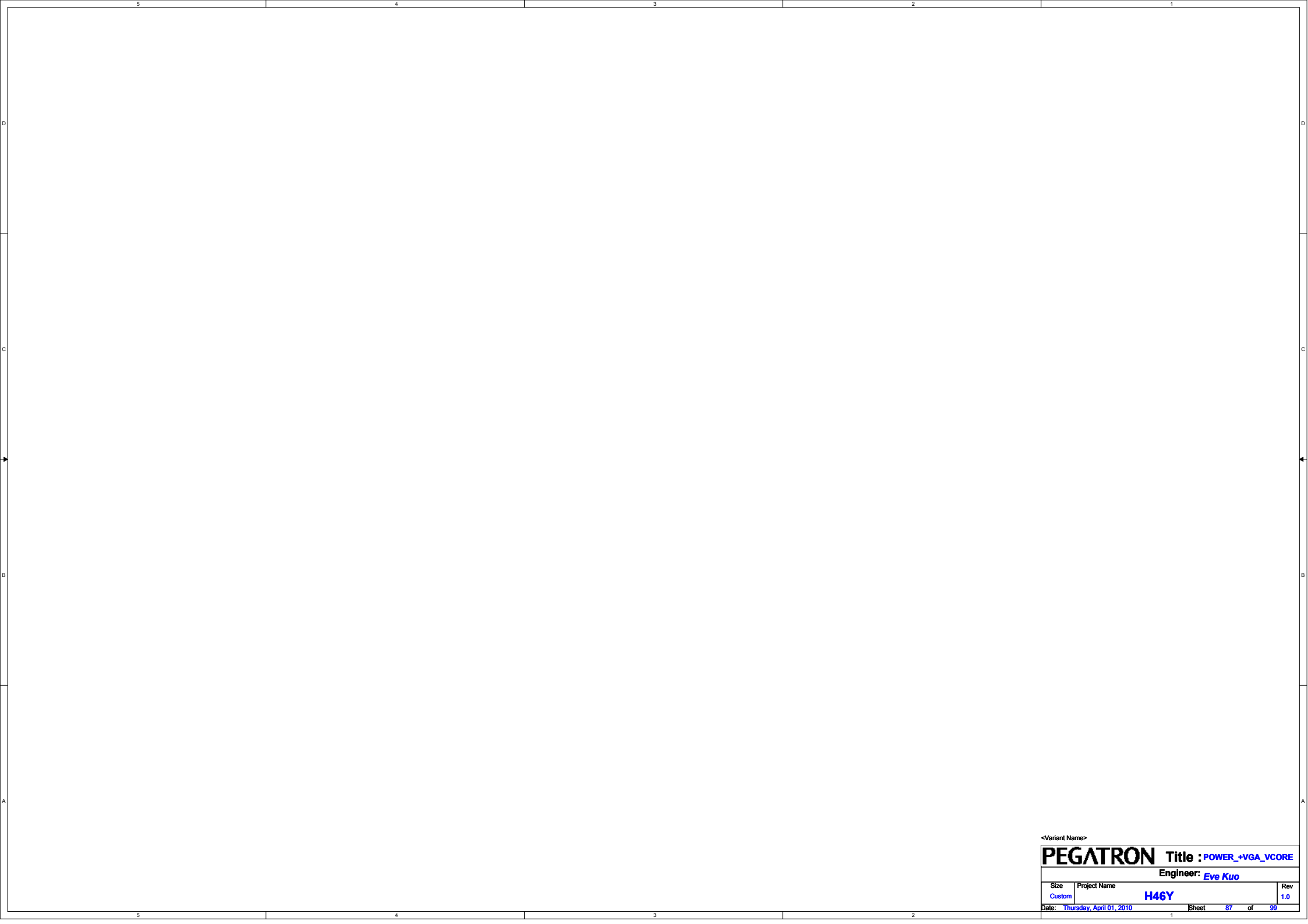






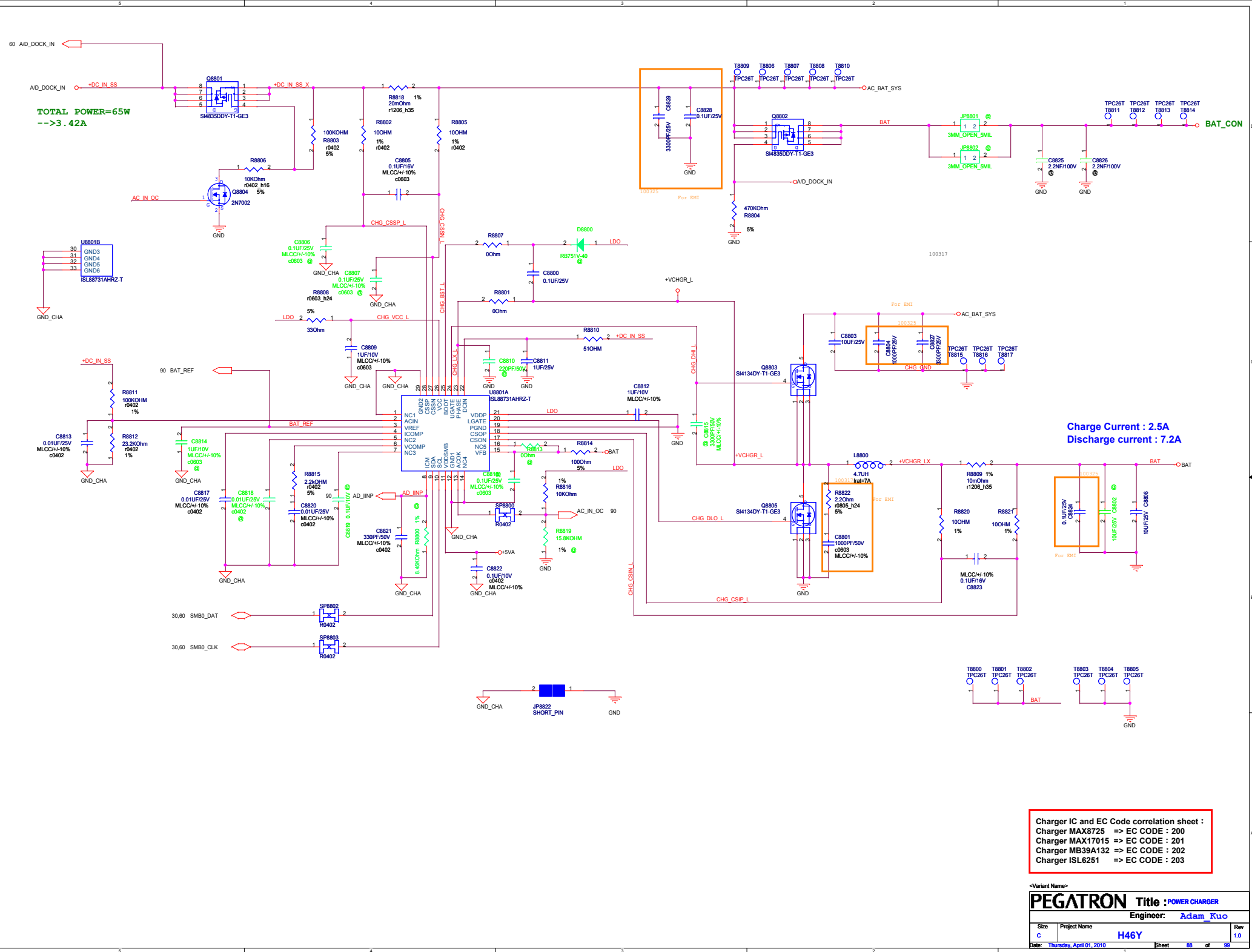




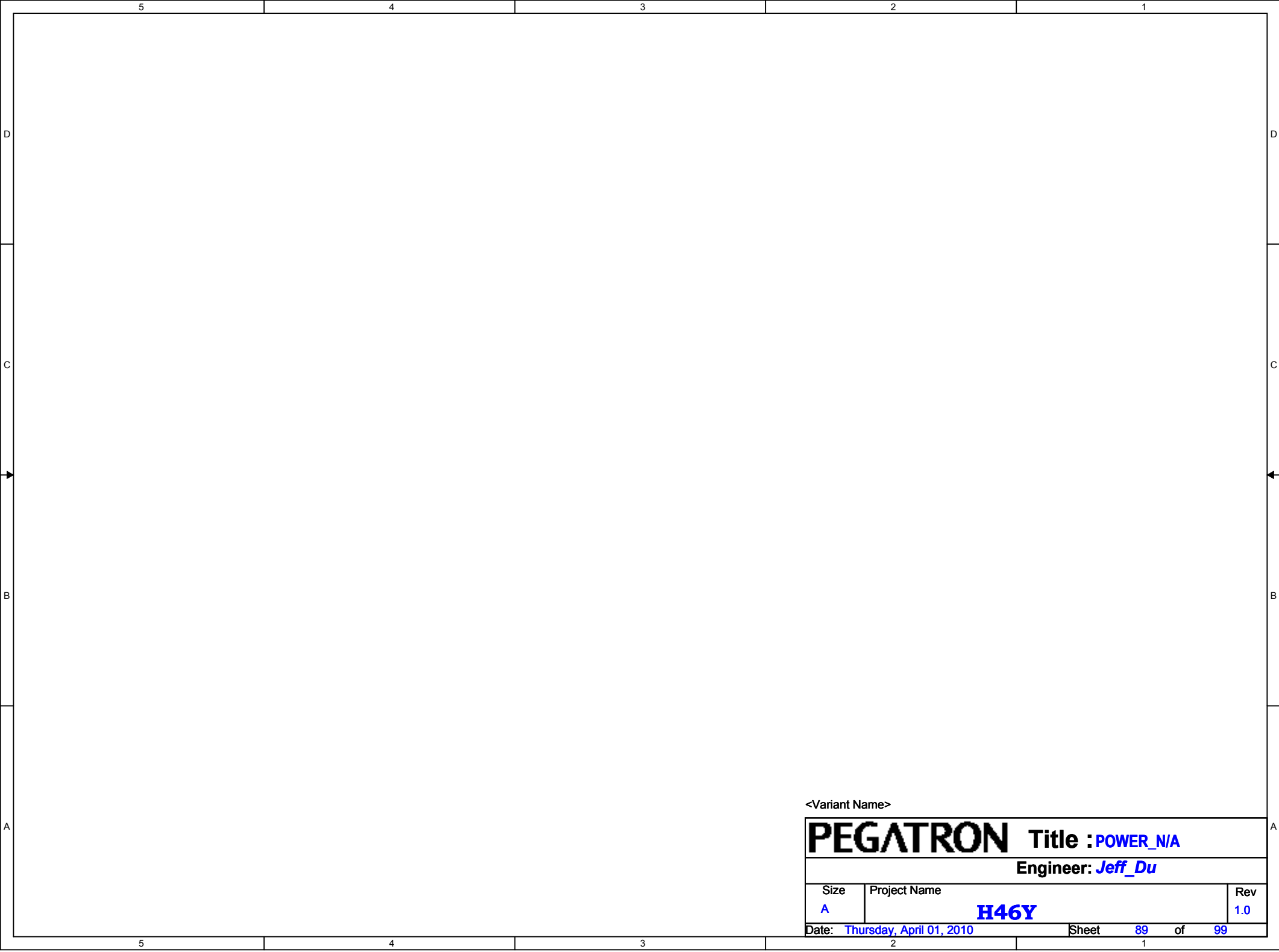


<Variant Name>

|                 |                          |                                 |                |
|-----------------|--------------------------|---------------------------------|----------------|
| <b>PEGATRON</b> |                          | <b>Title :</b> POWER_+VGA_VCORE |                |
|                 |                          | <b>Engineer:</b> Eve Kuo        |                |
| Size            | Project Name             |                                 | Rev            |
| Custom          | H46Y                     |                                 | 1.0            |
| Date:           | Thursday, April 01, 2010 |                                 | Sheet 87 of 99 |



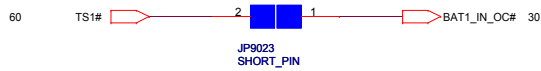
Charger IC and EC Code correlation sheet :  
Charger MAX8725 => EC CODE : 200  
Charger MAX17015 => EC CODE : 201  
Charger MB39A132 => EC CODE : 202  
Charger ISL6251 => EC CODE : 203



<Variant Name>

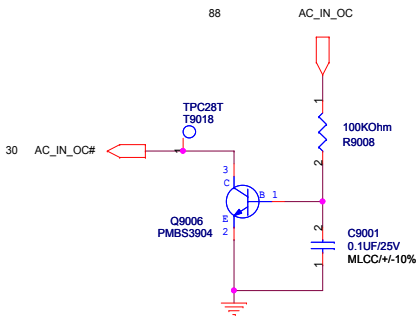
|                                       |                             |  |                          |           |                   |
|---------------------------------------|-----------------------------|--|--------------------------|-----------|-------------------|
| <b>PEGATRON</b>                       |                             |  | Title : <b>POWER_N/A</b> |           |                   |
| Engineer: <b>Jeff_Du</b>              |                             |  |                          |           |                   |
| Size<br><b>A</b>                      | Project Name<br><b>H46Y</b> |  |                          |           | Rev<br><b>1.0</b> |
| Date: <b>Thursday, April 01, 2010</b> |                             |  | Sheet                    | <b>89</b> | of <b>99</b>      |

BATTERY IN DETECT



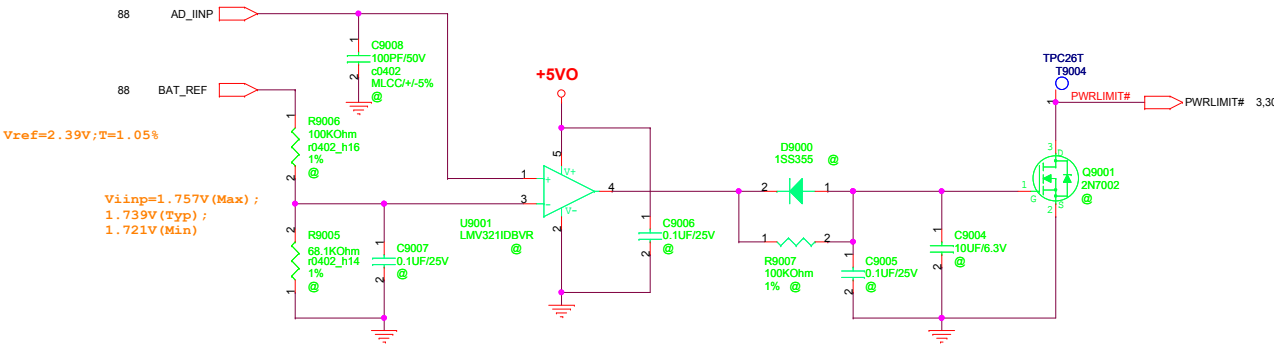
ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component



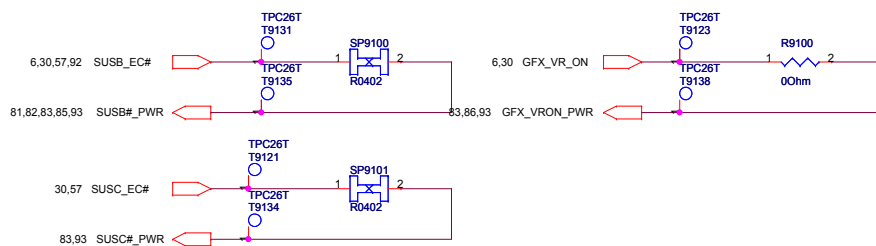
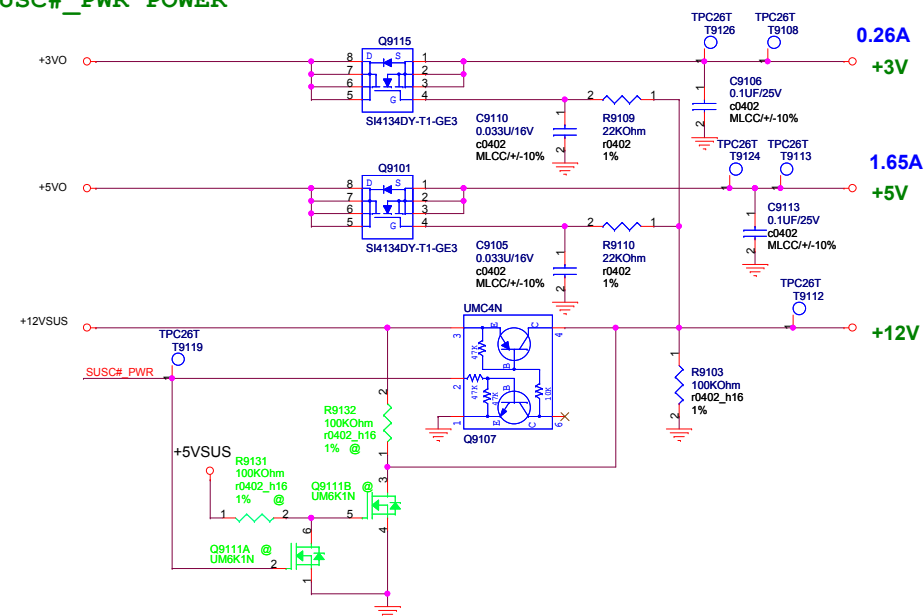
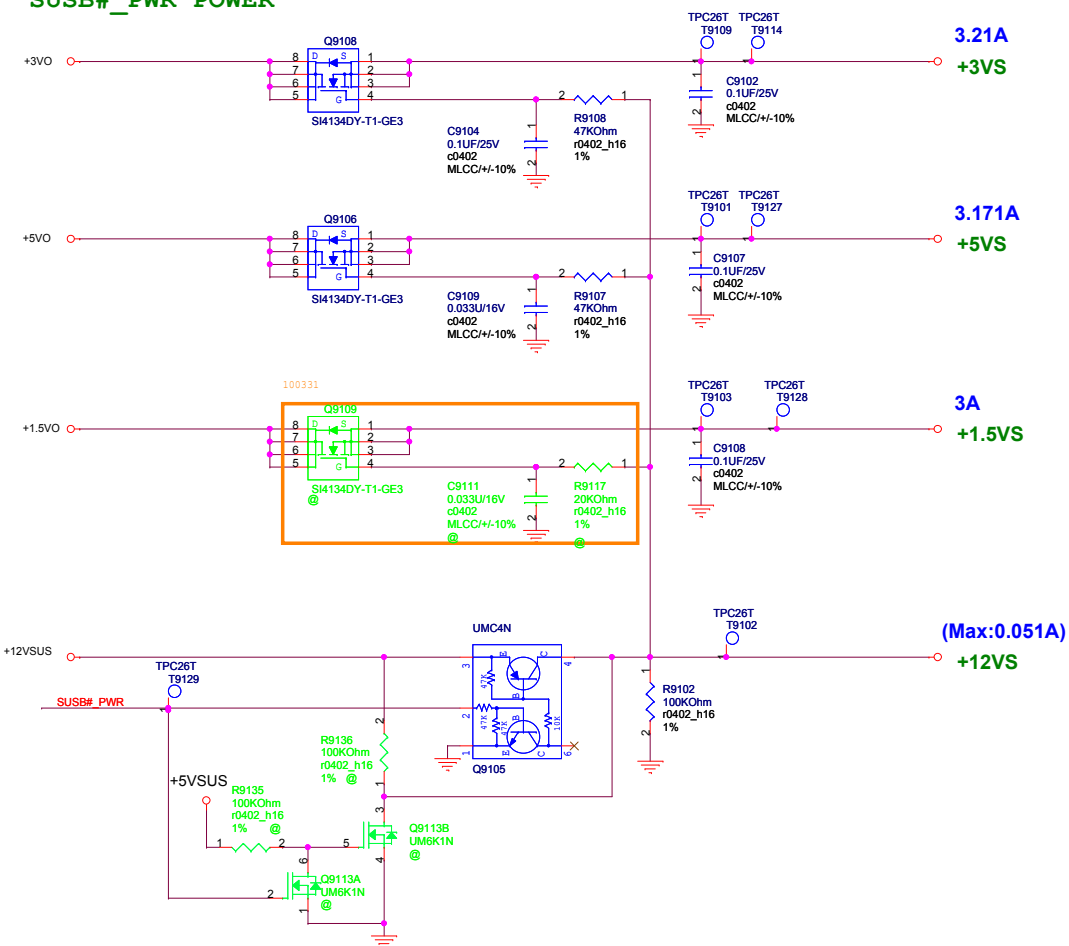
POWER LIMIT CIRCUIT

+2.5Vref delete



Pinput=65W----->Iinput=3.25A    R2=20 mohm  
Vicm=20\*Iinput\*R2 ==> Vicm=1.3655V(max)  
1.3V (typ)  
1.2355V(min))

| SUSB# | PWR | POWER |
|-------|-----|-------|
|-------|-----|-------|



**<Variant Name>**

PEGATRON Title : POWER\_LOAD SWITCH

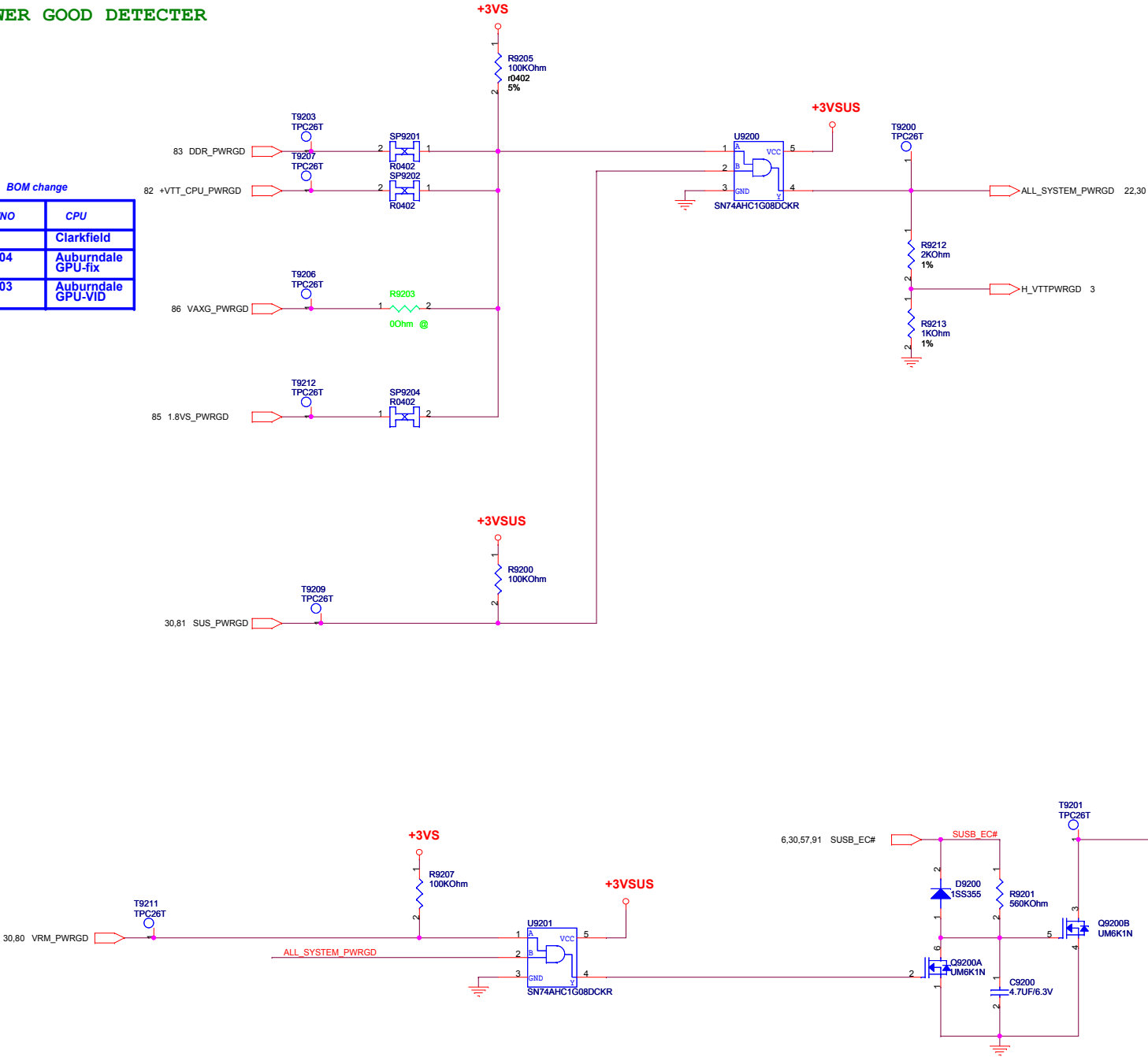
|                           |                             |                   |
|---------------------------|-----------------------------|-------------------|
| Engineer: <b>Adam_Kuo</b> |                             |                   |
| Size<br><b>Custom</b>     | Project Name<br><b>H46Y</b> | Rev<br><b>1.0</b> |

Date: Thursday, April 01, 2010 Sheet 91 of 99

POWER GOOD DETECTOR

BOM change

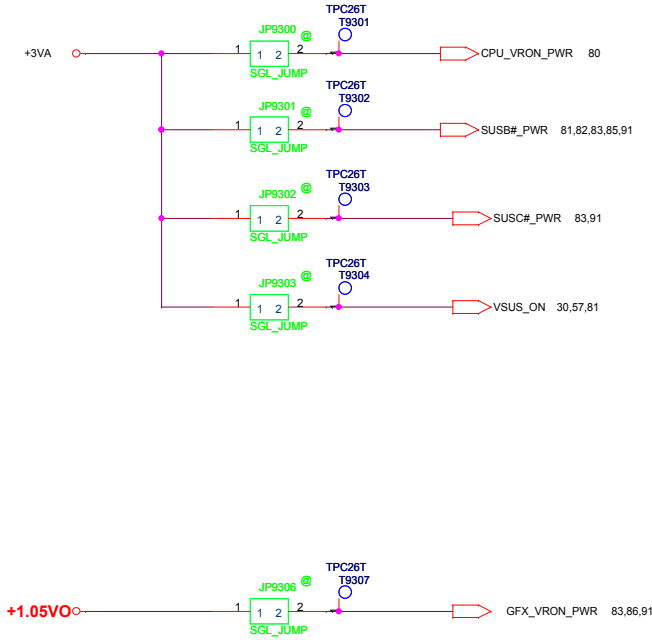
| YES/NO | CPU                |
|--------|--------------------|
| X      | Clarkfield         |
| R9204  | Auburndale GPU-fix |
| R9203  | Auburndale GPU-VID |



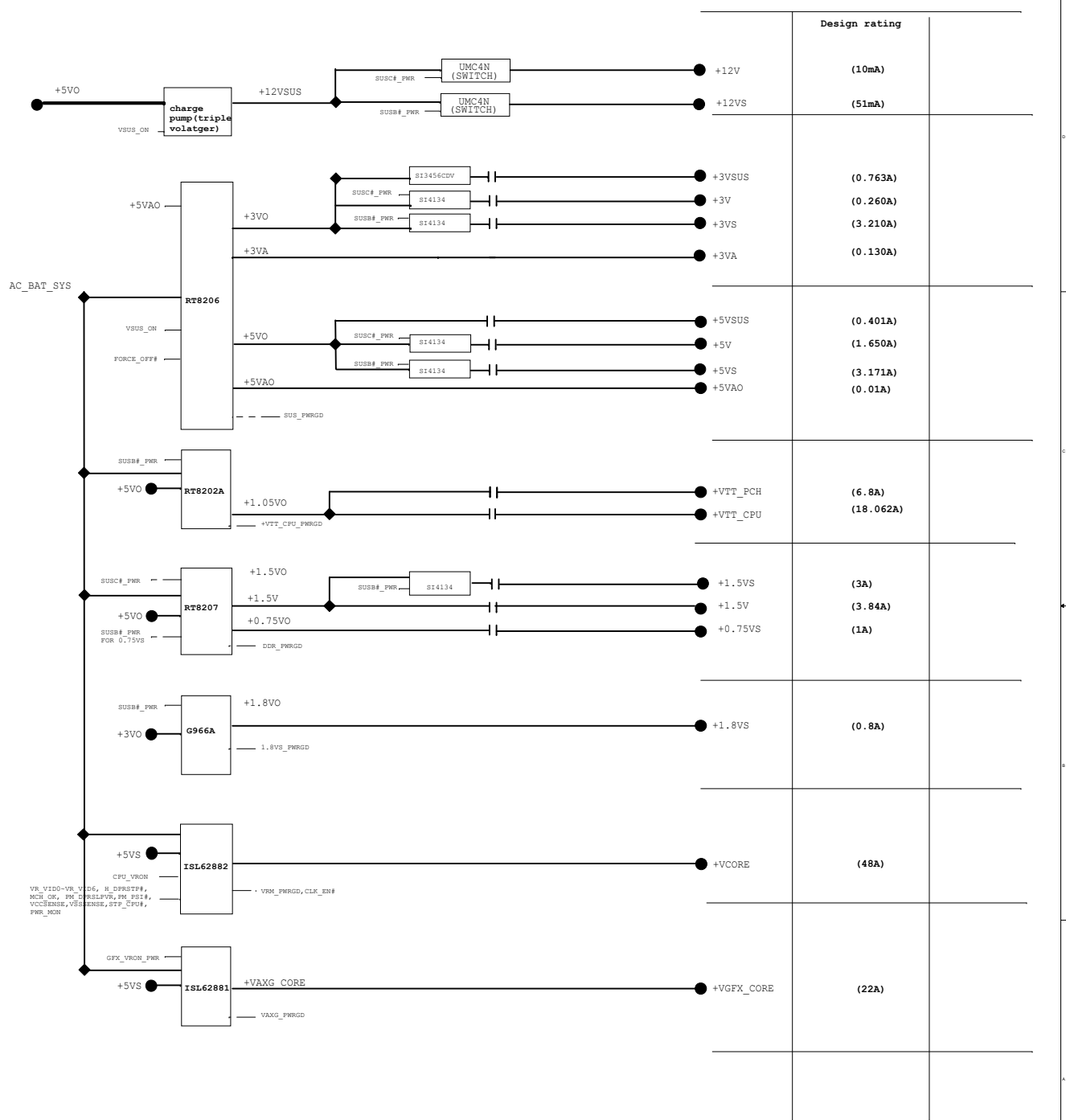
AC\_BAT\_SYS    AC\_BAT\_SYS    45,80,81,82,83,86,88  
BAT    BAT    88  
BAT\_CON    BAT\_CON    60,88

+3VA    +3VA    20,30,31,56,57,81  
+5VAO    +5VAO    81,85  
+5VA    +5VA    81,82,88  
  
+5VO    +5VO    81,82,83,90,91  
+3VO    +3VO    81,85,91  
+1.8VO    +1.8VO    85  
  
+1.05VO    +1.05VO    80,82,86  
  
+0.75VS    +0.75VS    7,8,57,83  
+1.5VO    +1.5VO    83,91  
+5VSUS    +5VSUS    27,81,83,91  
+3VSUS    +3VSUS    3,21,22,24,25,27,30,33,34,55,57,81,92  
+12VSUS    +12VSUS    55,81,83,91  
  
+5V    +5V    52,56,57,61,85,91  
+3V    +3V    3,24,30,40,44,53,54,56,57,91  
+12V    +12V    57,91  
  
+3VS    +3VS    3,7,8,20,21,22,23,24,25,26,27,28,29,30,32,45,46,47,50,51,53,54,55,56,57,80,86,91,92  
+1.5V    +1.5V    3,6,7,9,57,83  
  
+5VS    +5VS    27,30,31,46,47,50,51,55,57,80,86,91  
+12VS    +12VS    28,57,91  
+1.05VS    +1.05VS    26,27,29,57,80,82  
  
+VTT\_CPU    +VTT\_CPU    3,6,25,26,27,32,57,82  
  
+1.5VS    +1.5VS    6,57,91  
+1.8VS    +1.8VS    6,24,26,57,85  
  
+VCORE    +VCORE    6,57,80  
+VGFX\_CORE    +VGFX\_CORE    6,57,83,86

FOR POWER TEST

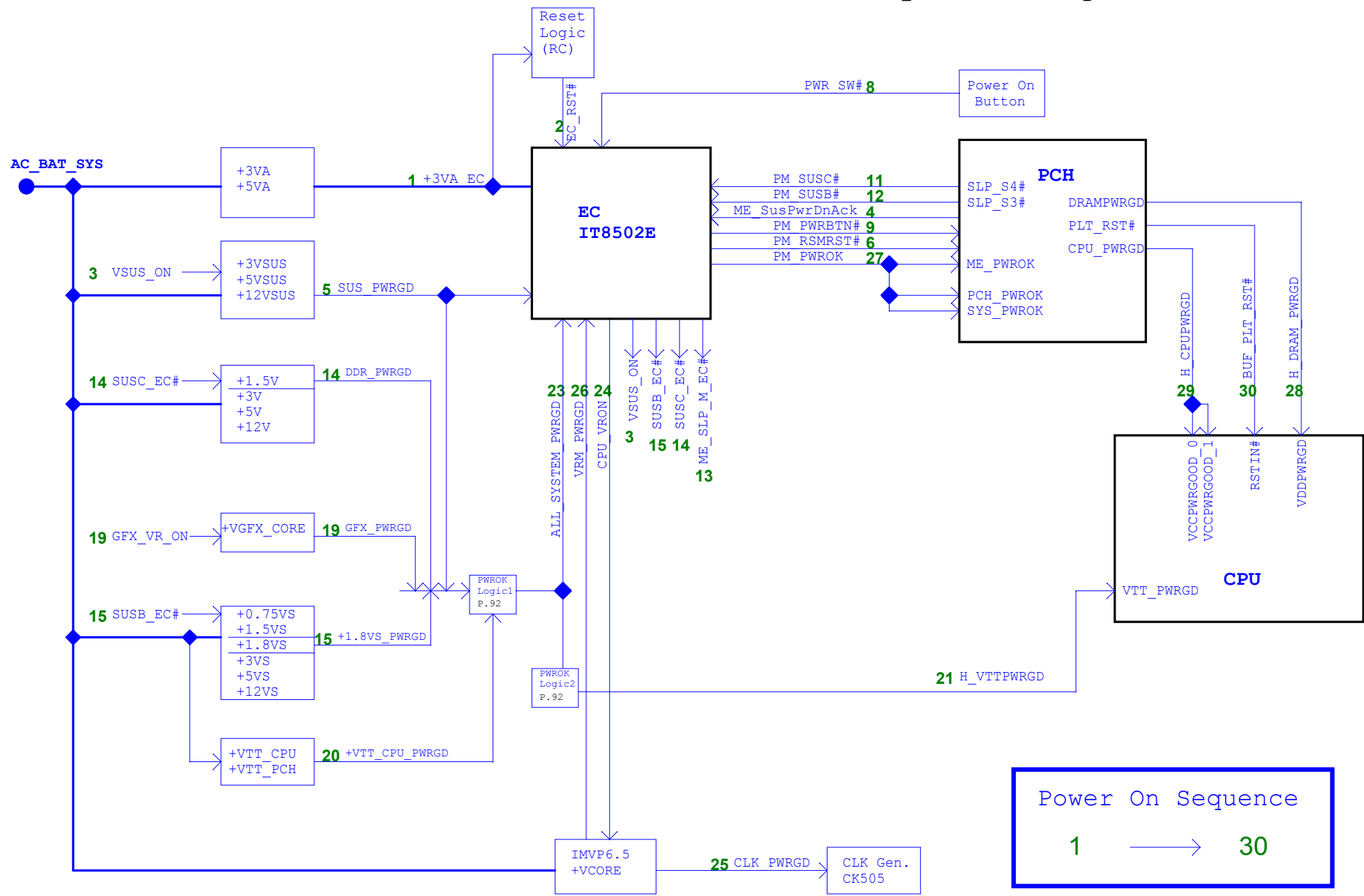








Power On Sequence Diagram Rev. 0.1



Power On Sequence  
1 → 30

# Power-On Sequence Timing Diagram Rev. 0.1

